

Compal Confidential

Cougar 2.0

Schematics Document

Intel Cedar Trail Processor/ Tiger point

2011-11-07

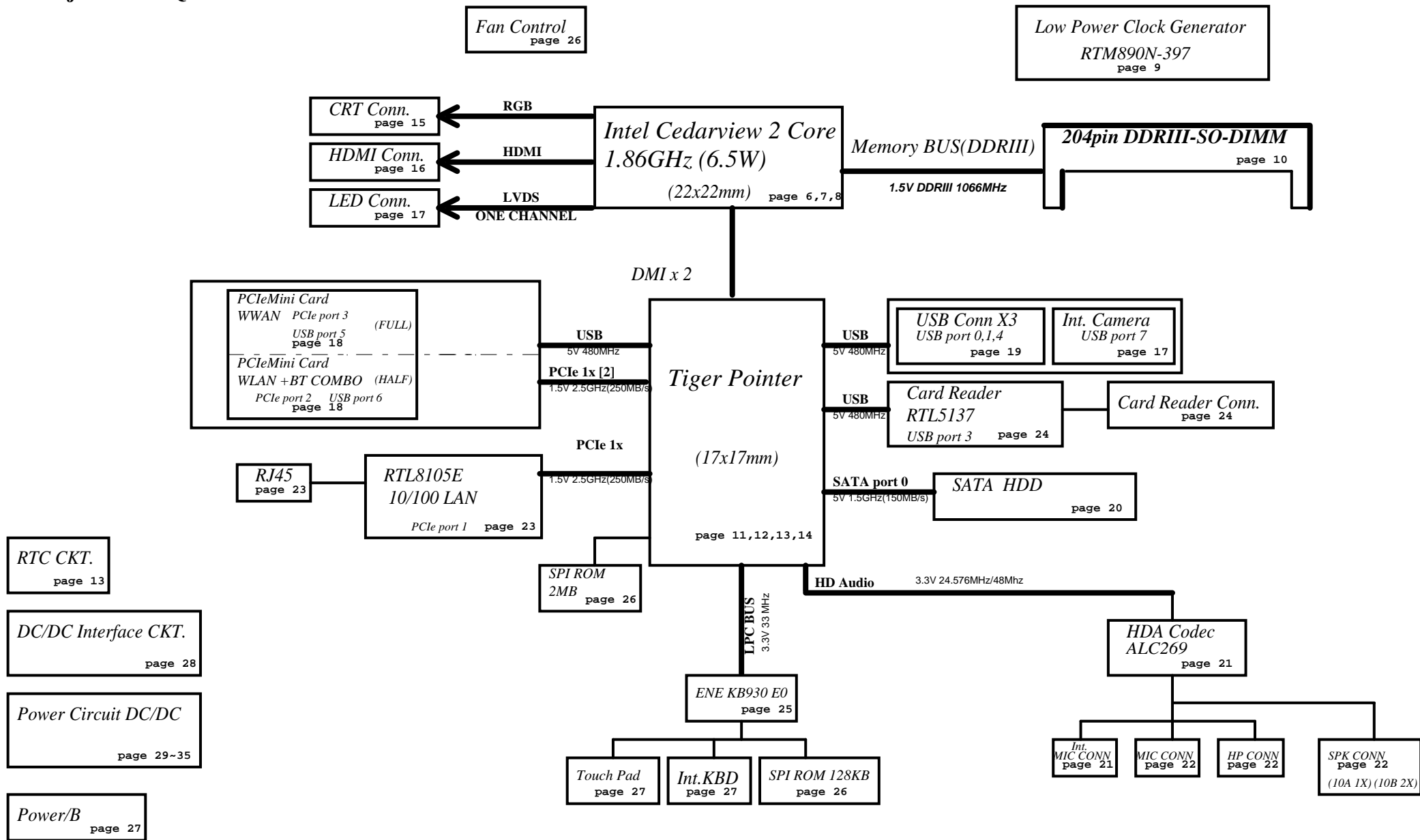
LA-6859P REV:1.0

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Model Name : Cougar 2.0

Project Code : QBU00



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+GFX_CORE	GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	OFF	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+3VS_PRIME	3.3V power rail for CPU and PCH	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT			Display		Clock gen	
description							
explain	Wi-Fi	WWAN	3G	CRT	HDMI	Tpye	
BTO	WLAN@	WWAN@	3G@	CRT@	HDMI@	low@	normal@

EC SM Bus1 address

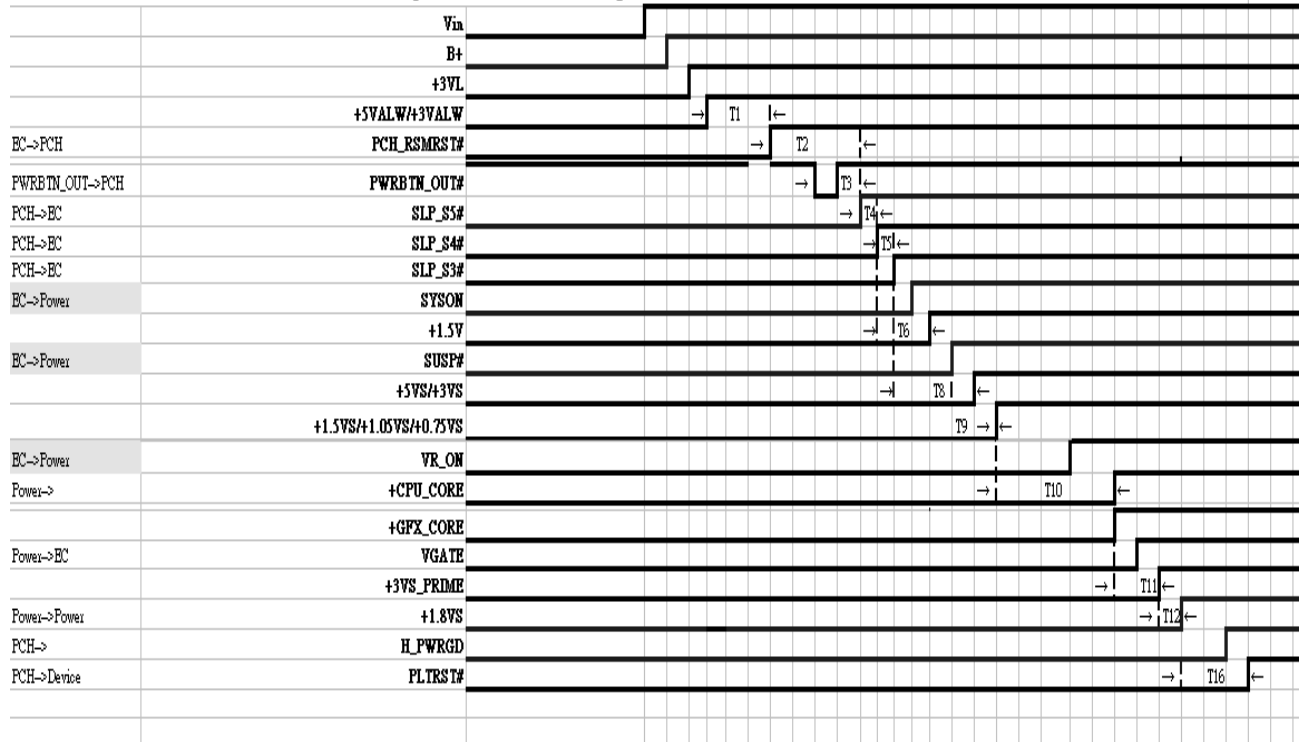
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

EC SM Bus2 address

NM10 SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

QBU00 Power ON sequence

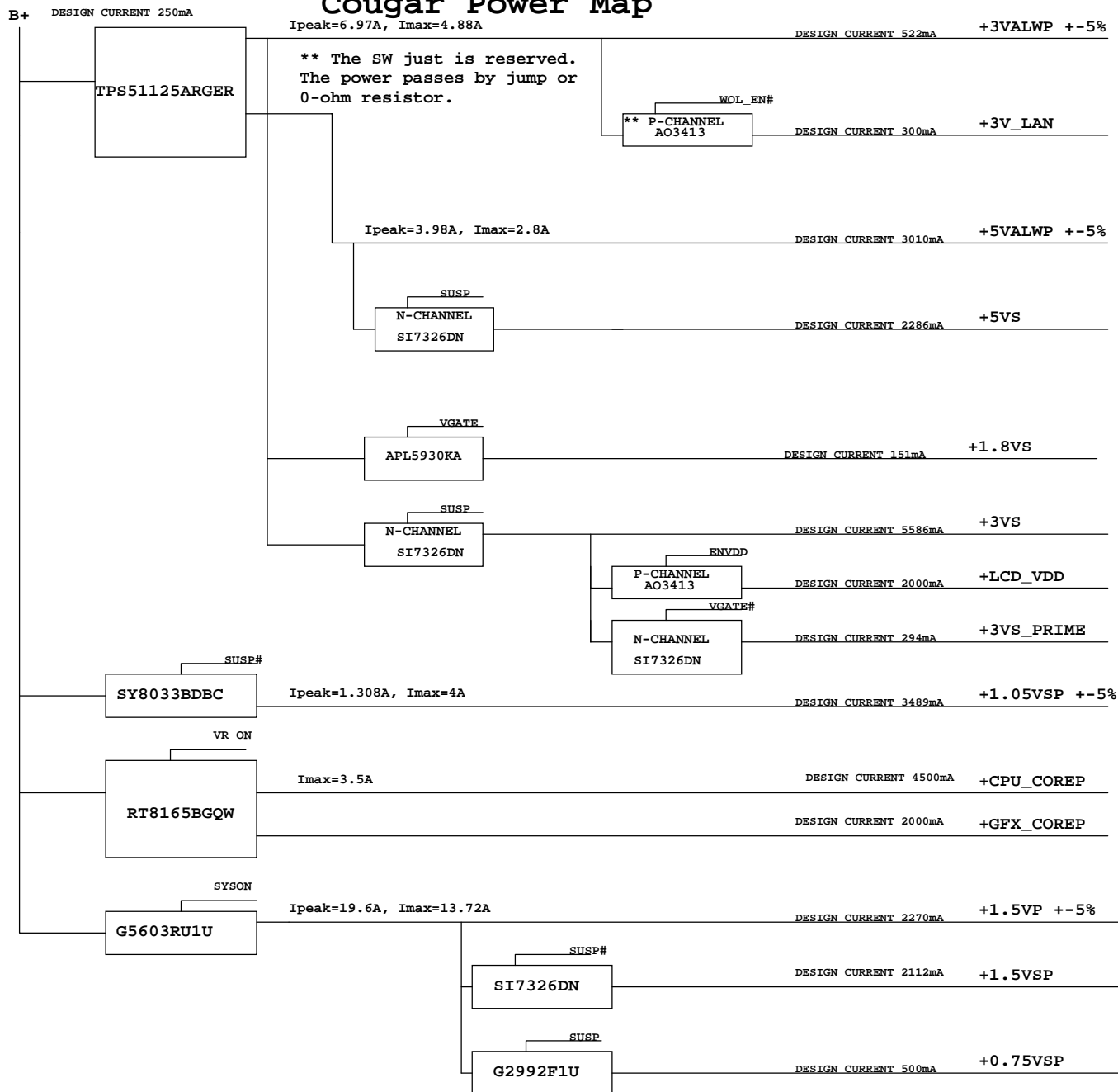


Power-on Sequence

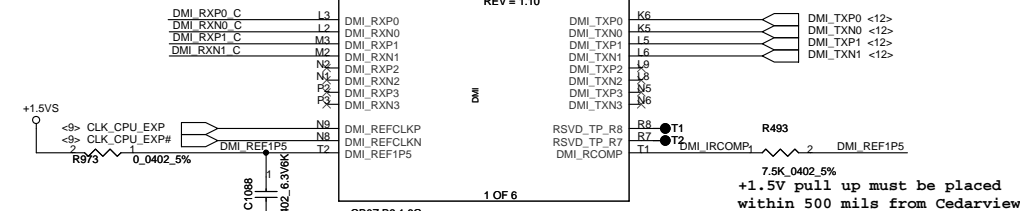
Time	Description	Expected
T1	+5V/3VALW to PCH_RSMRST# inactive	>0ms
T2	PCH_RSMRST# inactive to SLP_S5# inactive	<110ms
T3	PWRBTN_OUT# inactive to SLP_S5# inactive	>0ms
T4	SLP_S5# inactive to SLP_S4# inactive	28.992us ~ 64.088us
T5	SLP_S4# inactive to SLP_S3# inactive	28.992us ~ 64.088us
T6	SLP_S4# inactive to +1.5V active	>0ms
T8	SLP_S3# inactive to +5VS inactive	>0ms
T9	+1.5VS active to +1.05VS active	>0ms
T10	-1.05VS active to +CPU_CORE	>0ms
T11	+CPU_CORE active to +3.3V PRIME	>0ms
T12	+3.3V PRIME active to +1.8VS	3.3-1.8<700mV
T16	H_PWRGD inactive to PLTRST# inactive	34<RTCCLK<41

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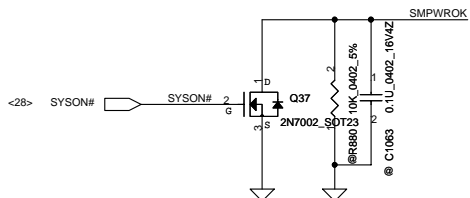
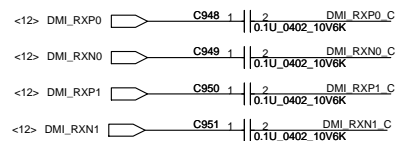
Cougar Power Map



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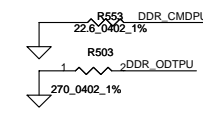
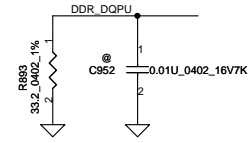
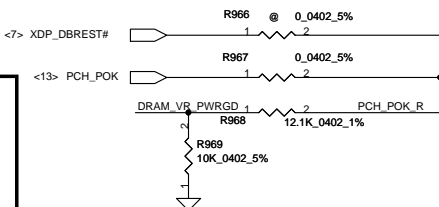
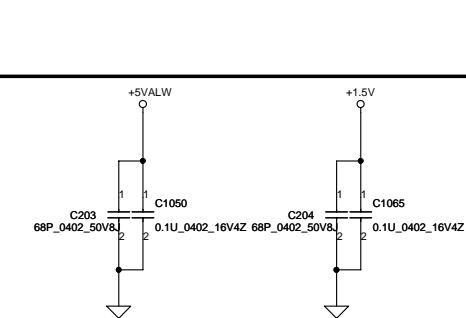
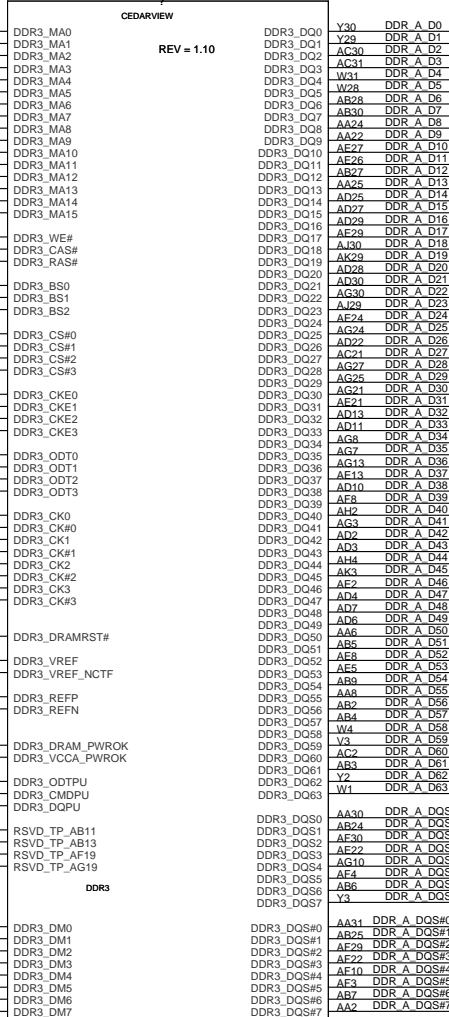
+1.5V pull up must be placed within 500 mils from Cedarview



<10> DDR_A_MA[0..15]
<10> DDR_A_DQS[0..7]
<10> DDR_A_DM[0..7]
<10> DDR_A_DQS[0..7]
<10> DDR_A_D[0..63]

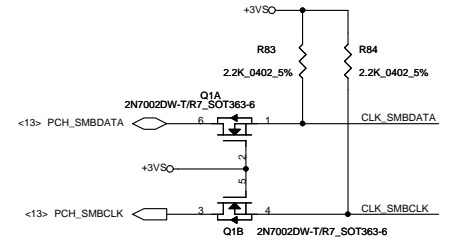
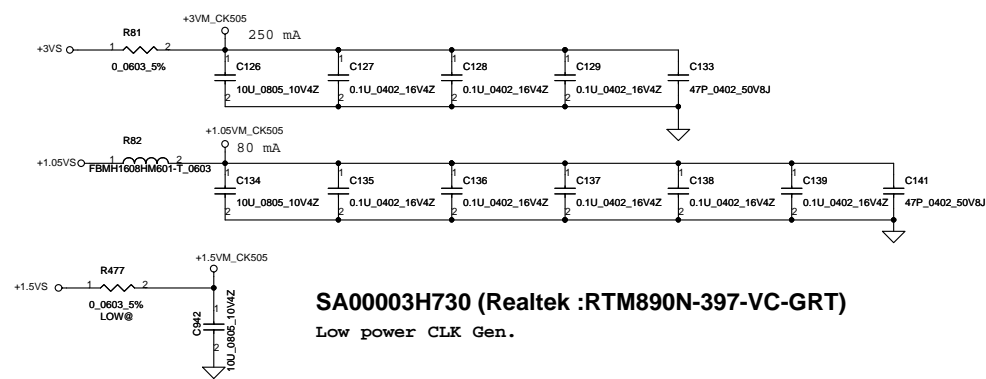
N2800@
U1
QB0Y B2 1.86G

U1B N2600@

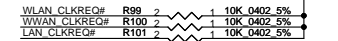


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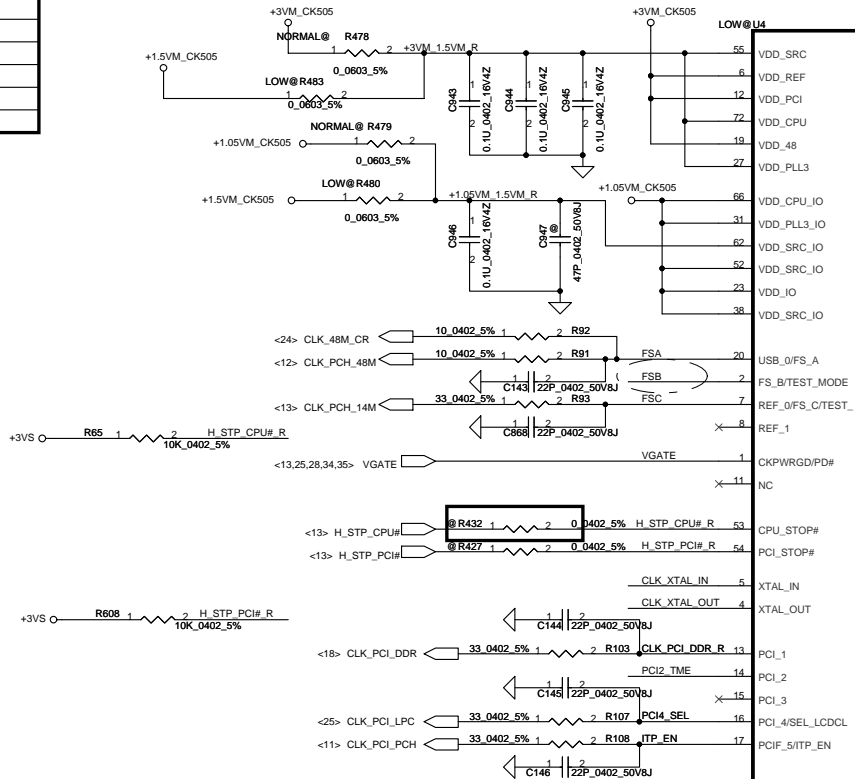
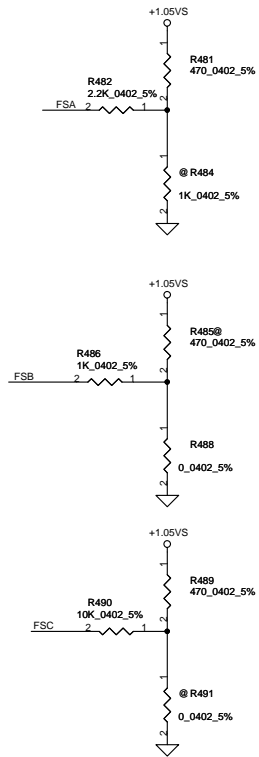
	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff



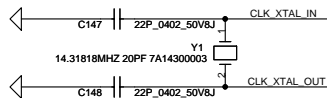
PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	
SRC3	CPU_EXP
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN



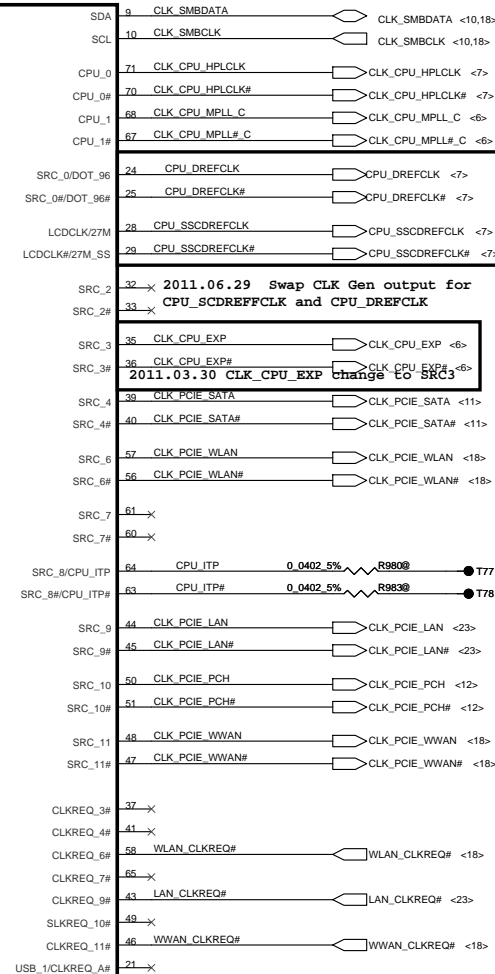
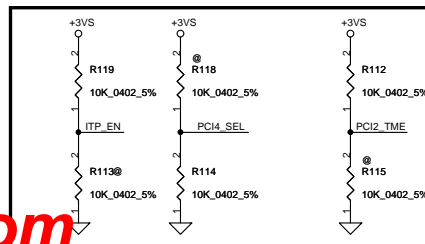
PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	



```
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
                  Pin28/29 : LCDCLK / LCDCLK#
                  1 = Pin24/25 : SRC_0 / SRC_0#
                  Pin28/29 : 27M/27M_SS
For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed
```



Routing the trace at least 10mil



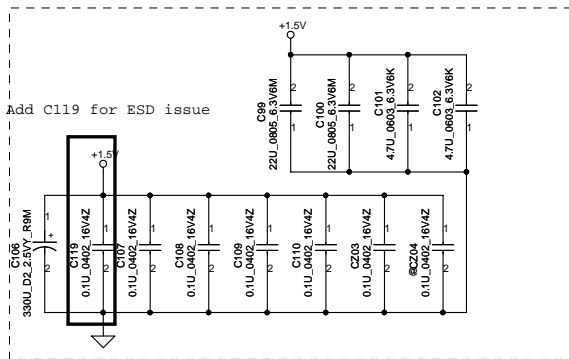
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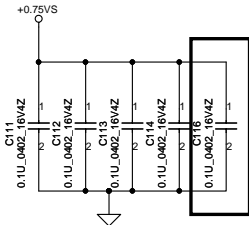
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 <6> DDR_A_D[0..63]
 <6> DDR_A_DM[0..7]
 <6> DDR_A_DQS[0..7]
 <6> DDR_A_MA[0..15]

Layout Note:
Place near JDDR1

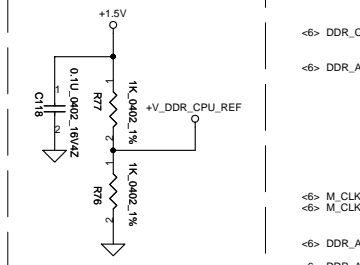
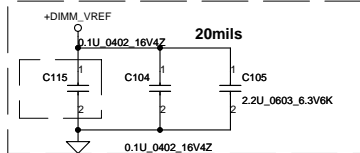
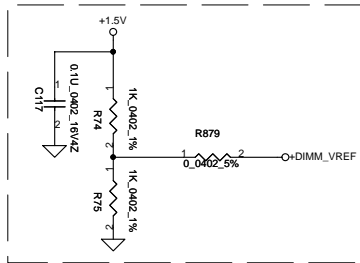
2011.06.14 Add C119 for ESD issue



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.75VS

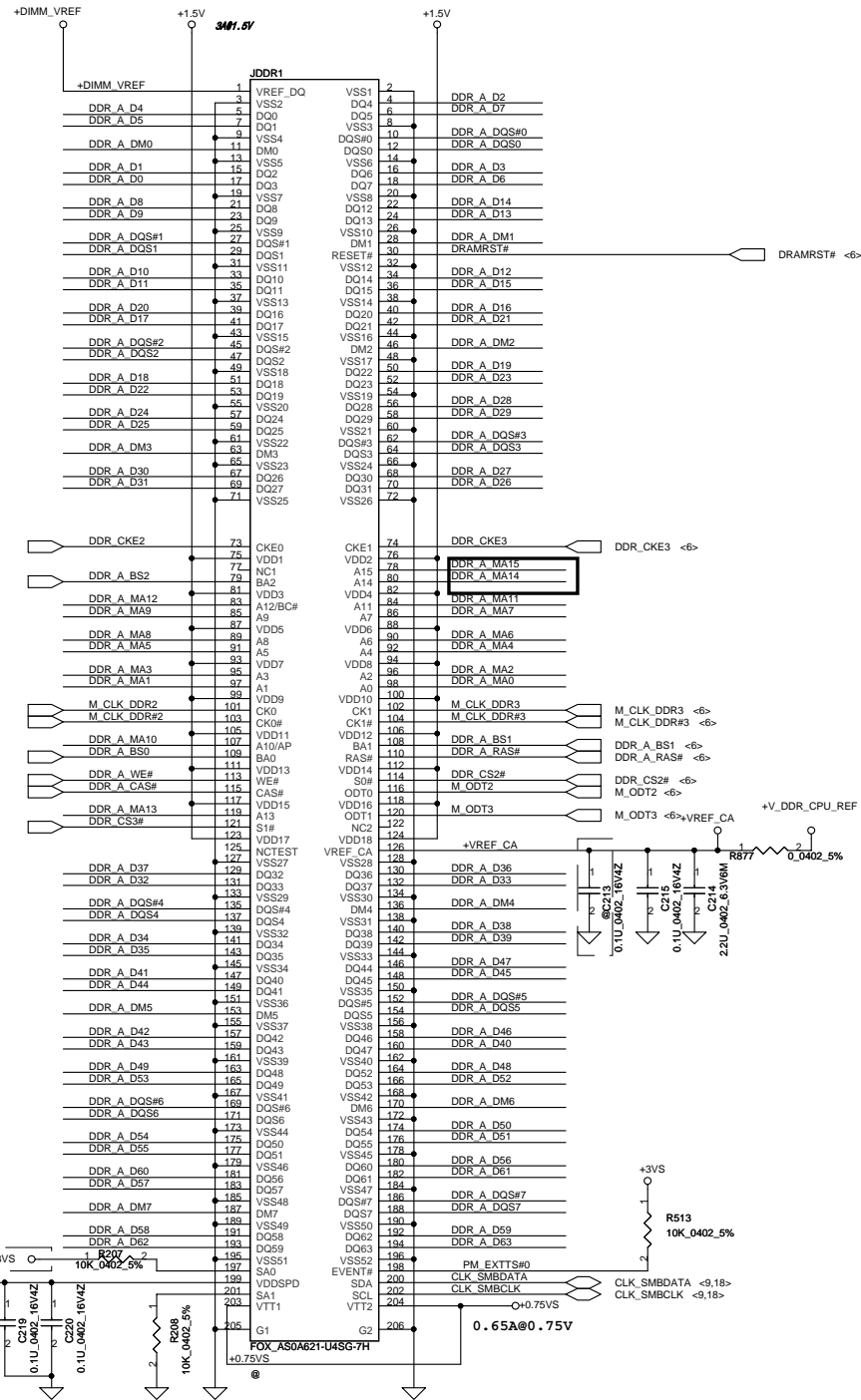
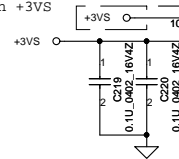


2011.06.14 Add C116 for ESD issue

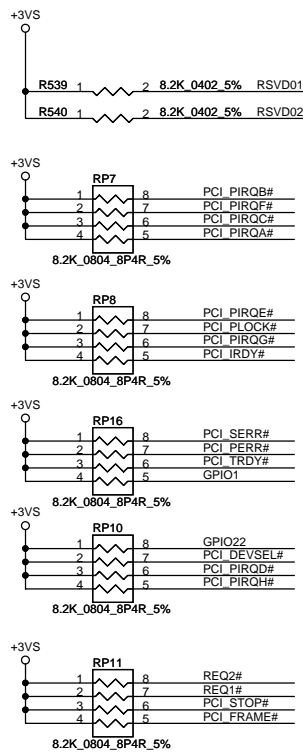


<6> DDR_CKE2
 <6> DDR_A_BS2
 <6> M_CLK_DDR2
 <6> M_CLK_DDR#2
 <6> DDR_A_BS0
 <6> DDR_A_WE#
 <6> DDR_A_CAS#
 <6> DDR_CS#

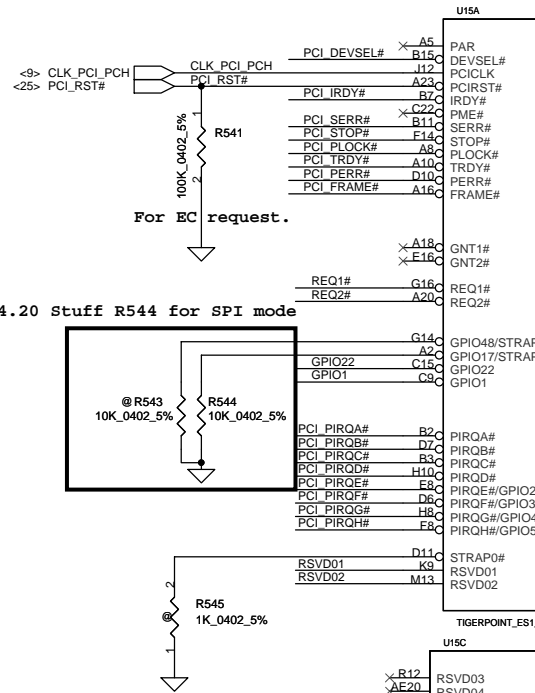
DVT# SA0 change to pull high +3VS



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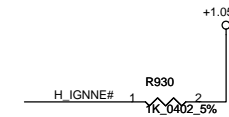
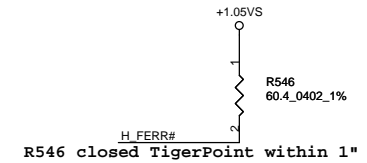
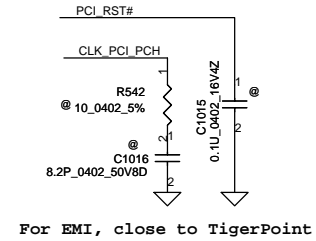
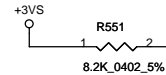


2011.04.20 Stuff R544 for SPI mode



Signals have weak internal pull-ups

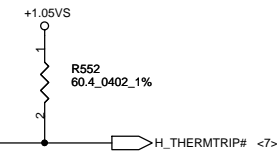
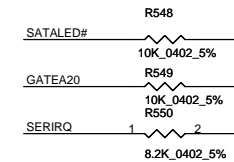
	GPIO17	GPIO48
SPI	0	1
PCI	1	0
LPC	1	1



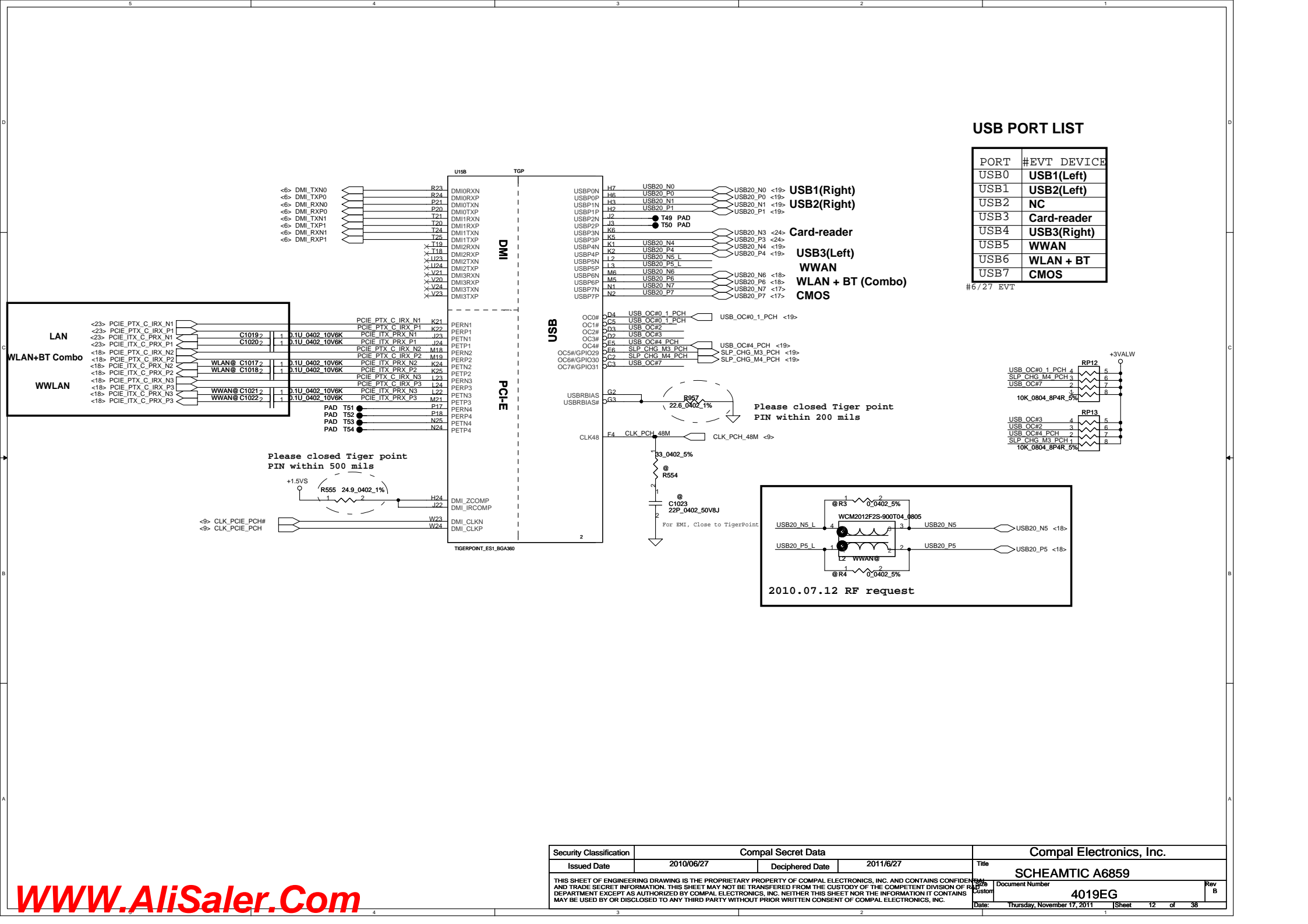
SATA

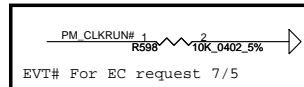
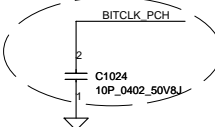
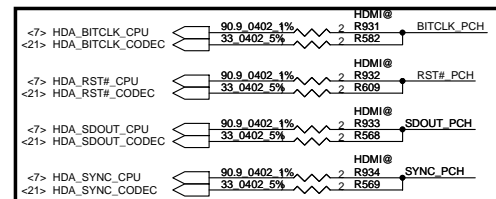
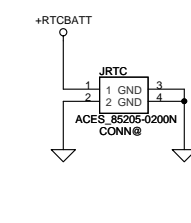
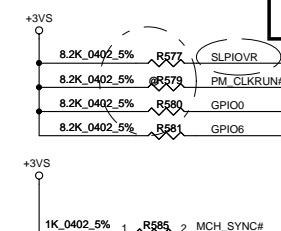
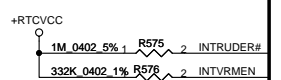
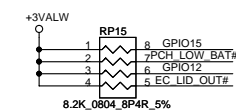
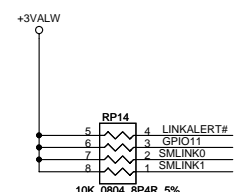
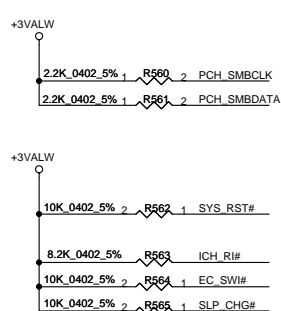
HOST

Please closed Tiger point PIN within 500 mils

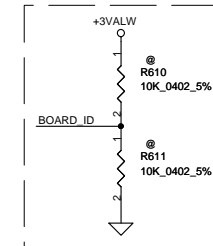
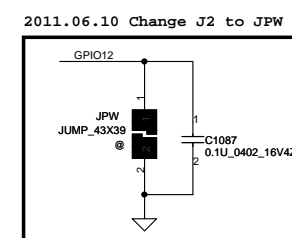


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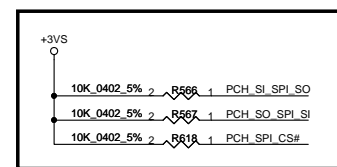
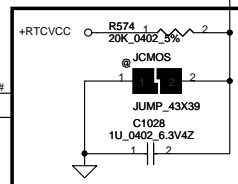




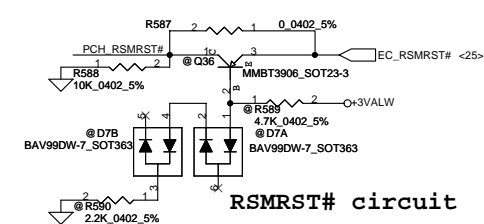
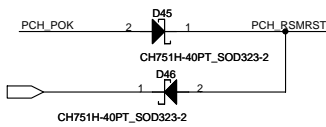
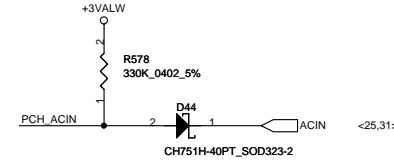
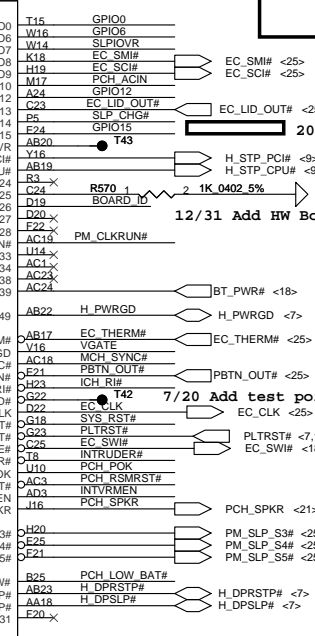
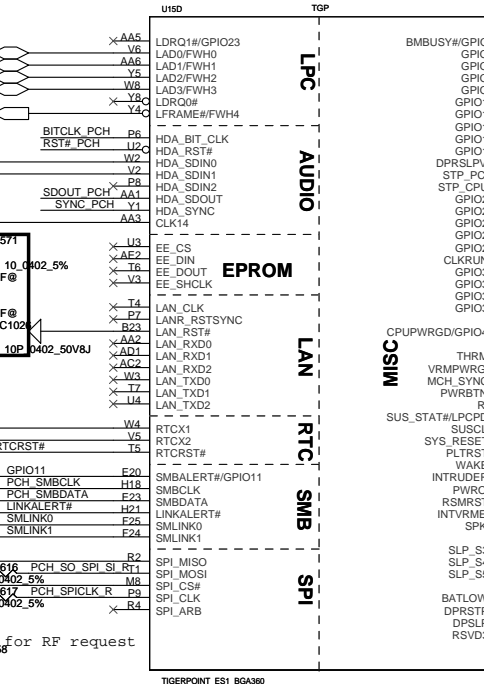
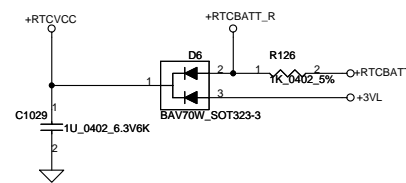
2011.04.26 Reserve GPIO12 for clean password
Layout note: Put J2 close to J1



2011.06.10 Change J1 to JCMOS

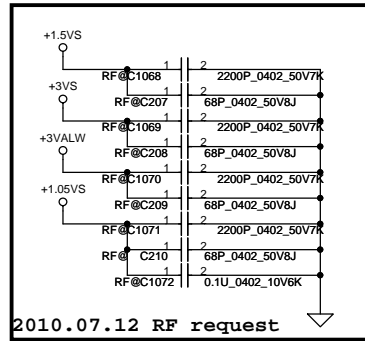
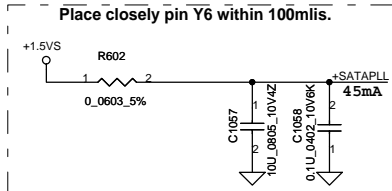
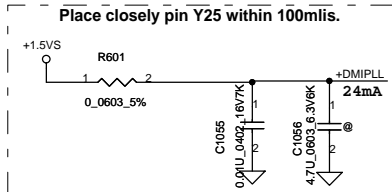
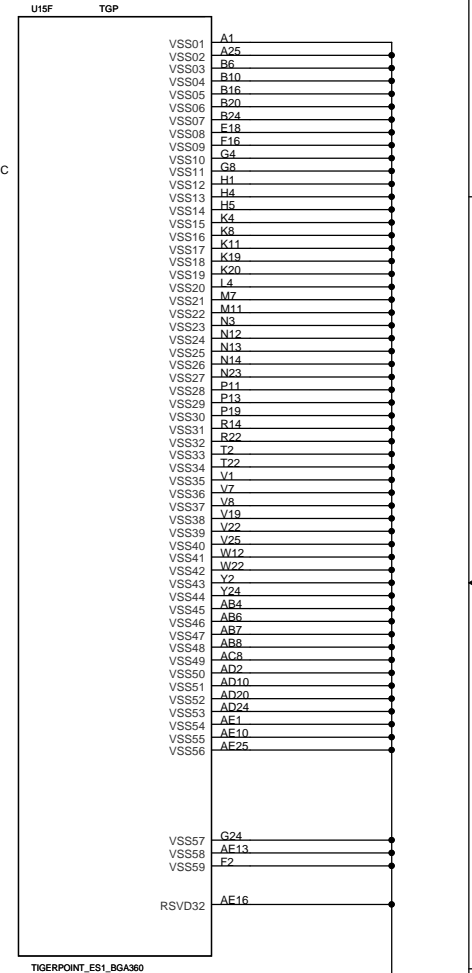
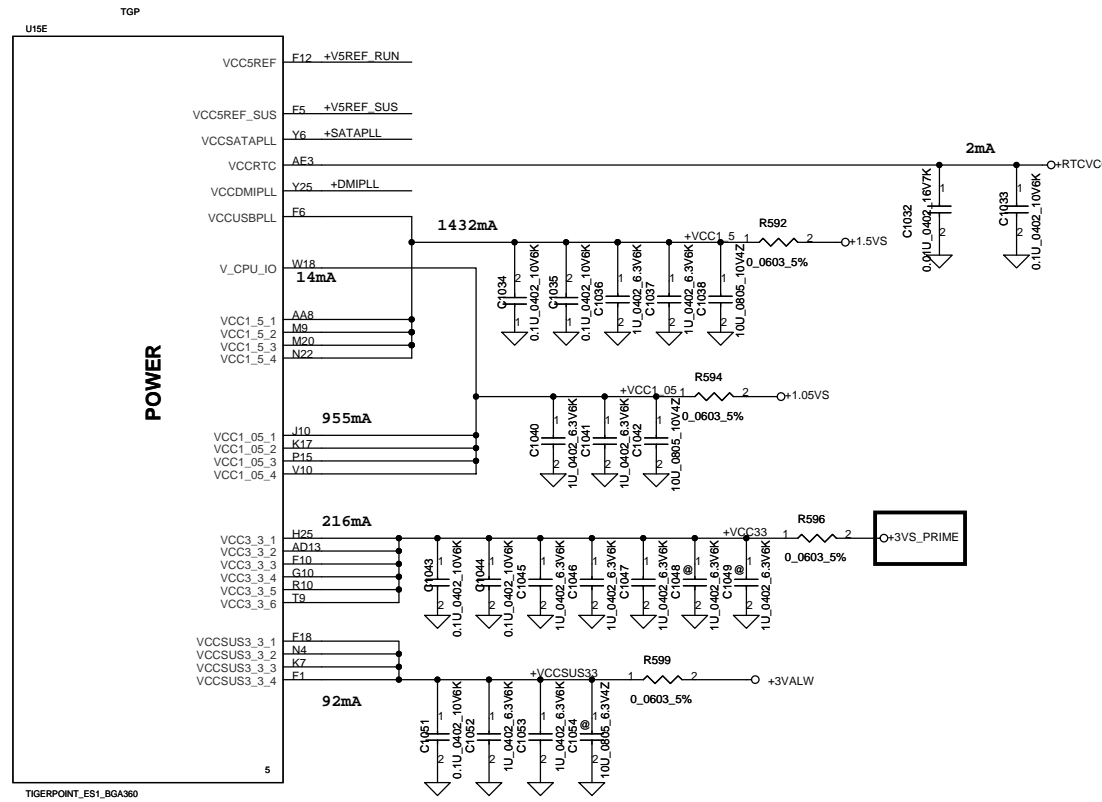
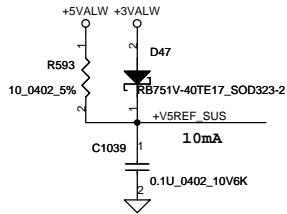
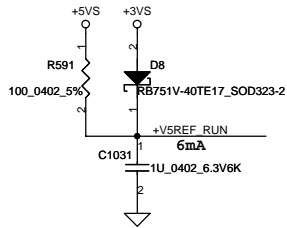


2011.06.15 Change Pull high to +3VS



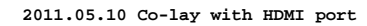
RSMRST# circuit

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				Document Number				4019EG			
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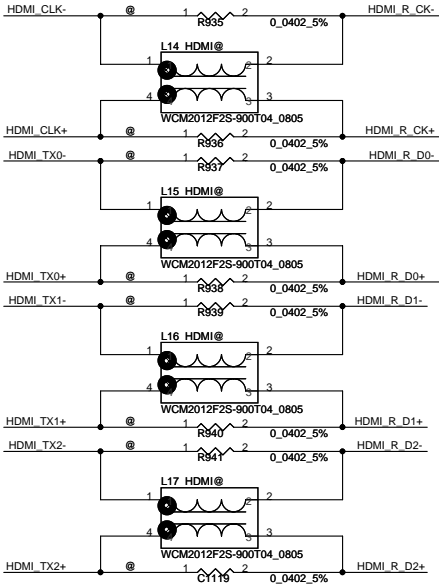
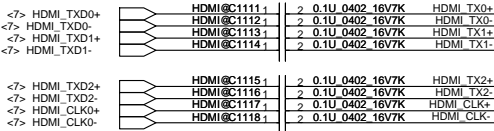
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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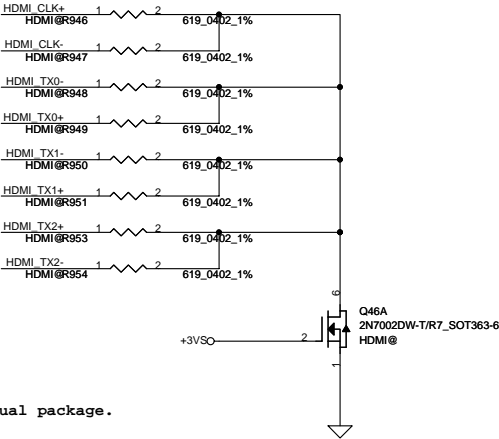
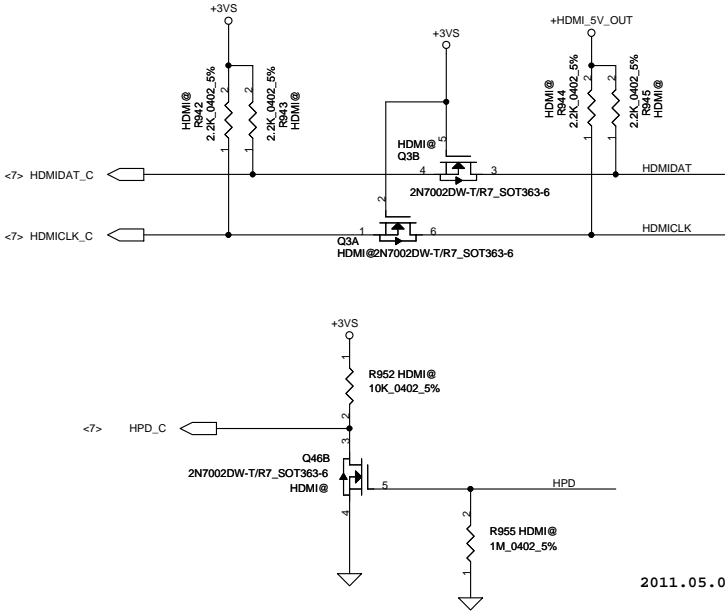
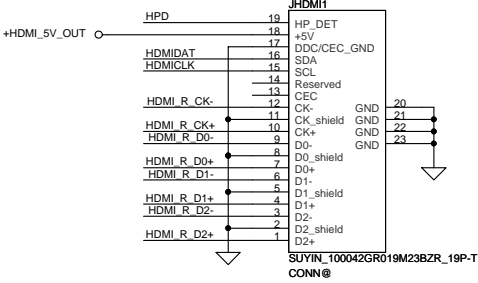


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HDMI CONNECTOR



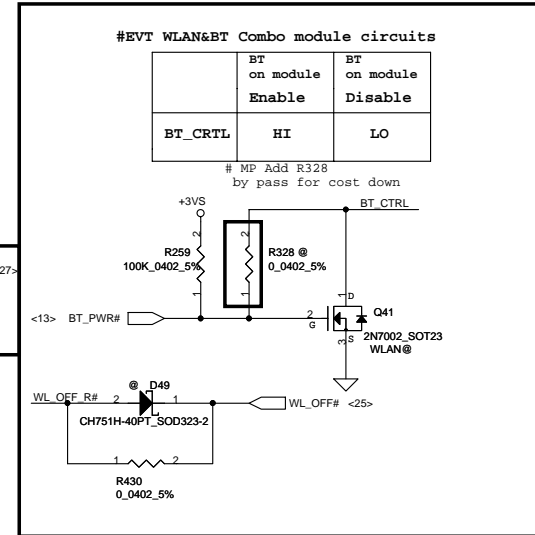
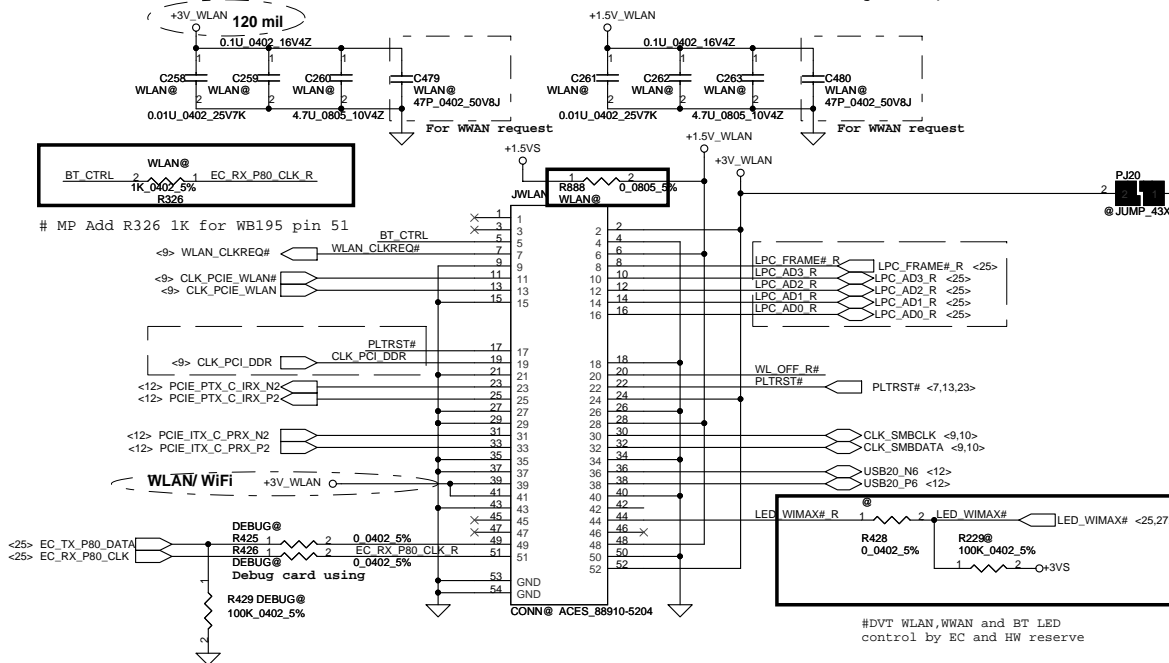
< HDMI Connector >



2011.05.04 Change Q42,Q43 to dual package.

Mini-Express Card for WLAN/WiMax

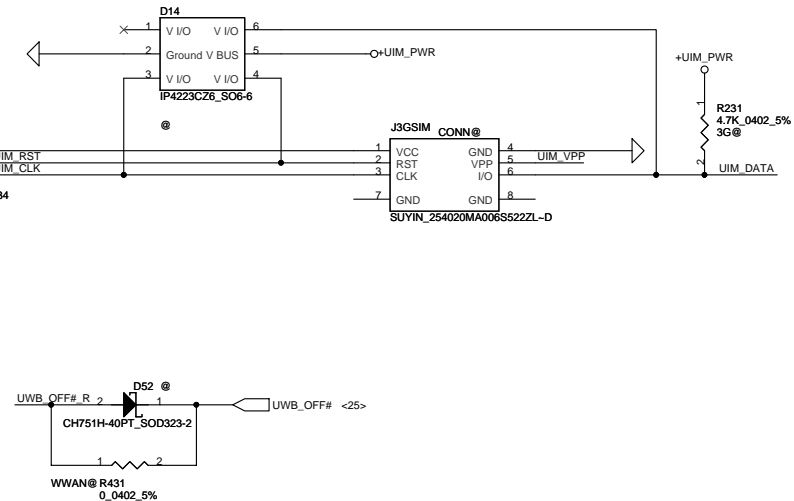
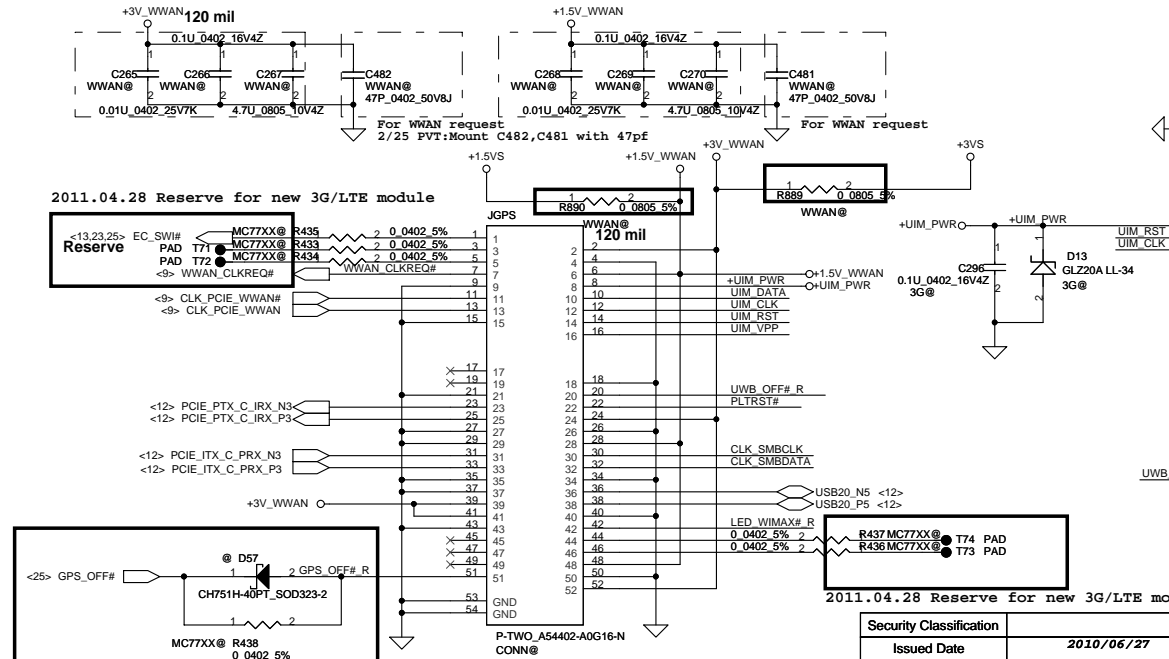
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@



Mini-Express Card for 3G/GPS

3G current need to 2750mA

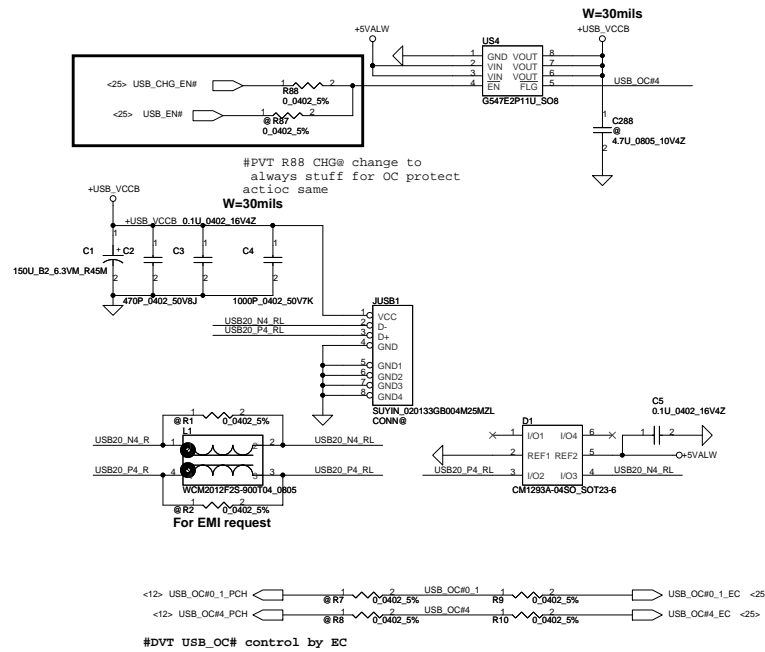
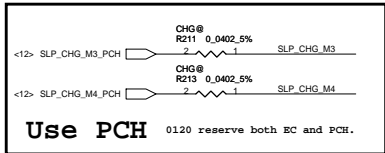
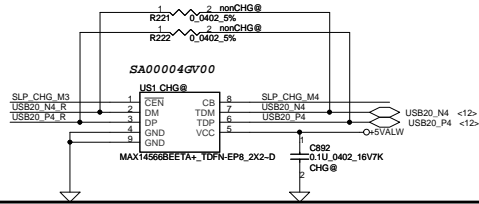
3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@



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USB Sleep & Charge Auto-Mode Mode3

MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

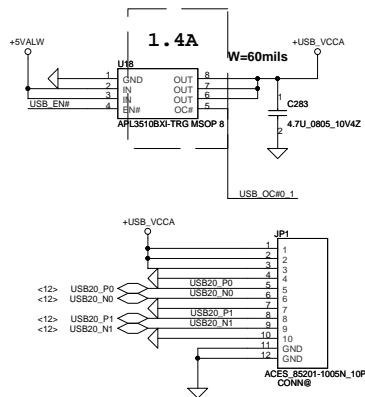


For EMI request

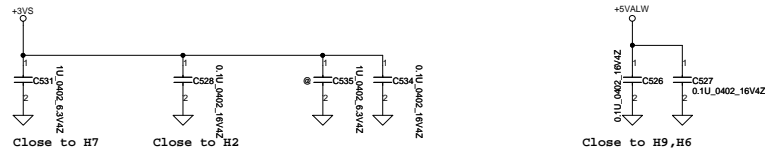
2/3 DVT: Change D38,D37 from PRT85V0U2X_SOT143-4 to CM1293A-0460_SOT23-6

For EMI request

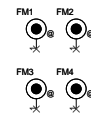
USB CONN



Add 0.1u Caps for each screw hole for ESD rule

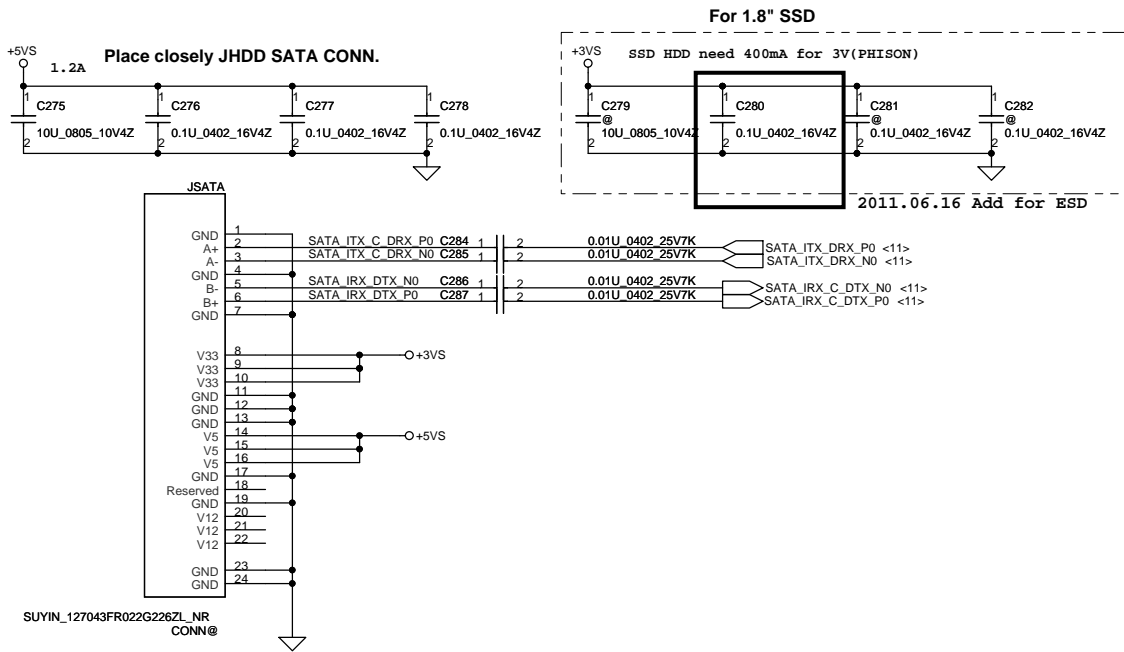


FIDUCIAL_C40M80



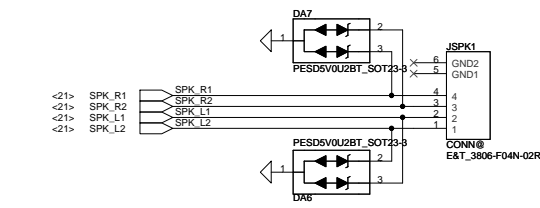
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SATA Conn.

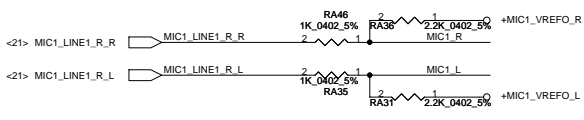


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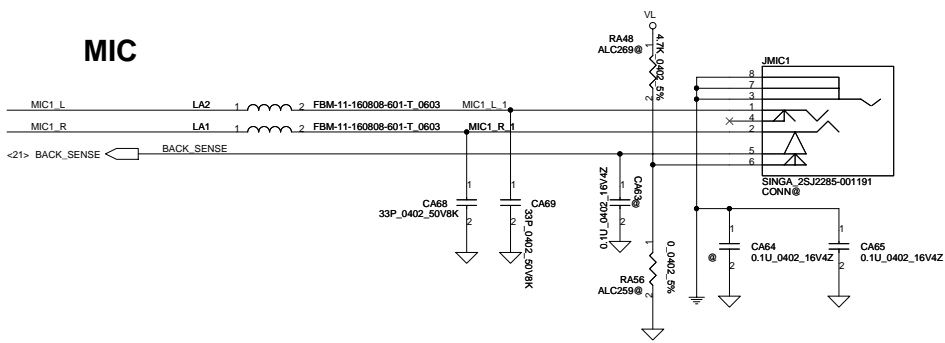
SPEAKER



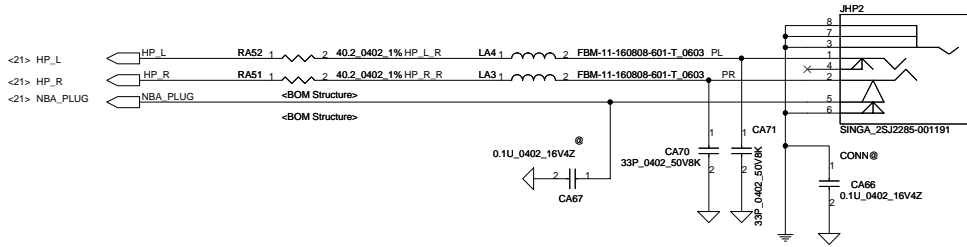
Ext.MIC/LINE IN JACK



MIC

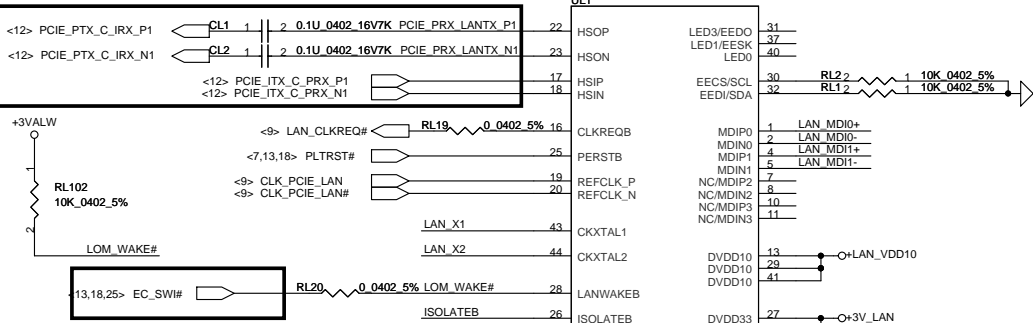


Head phone

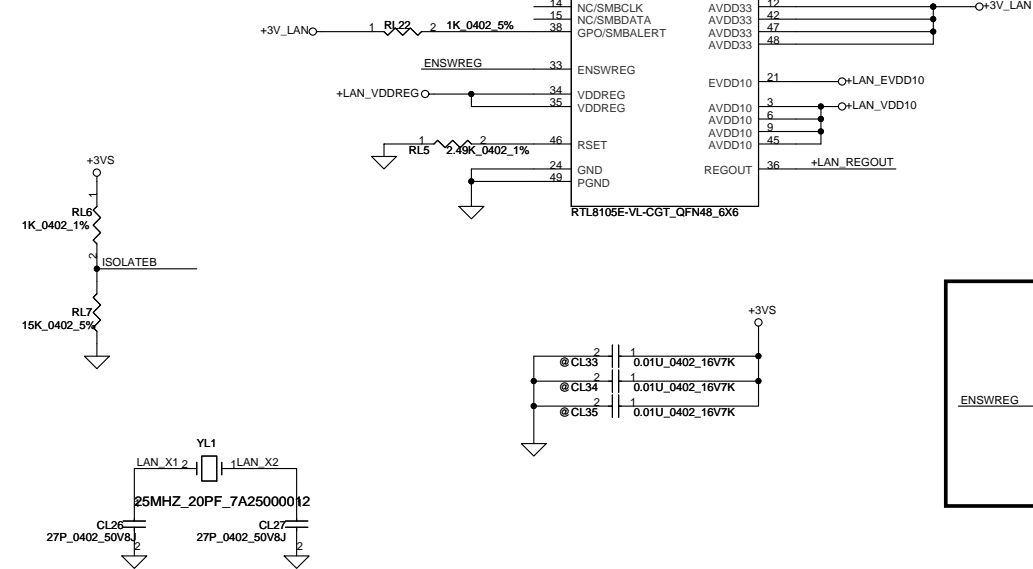


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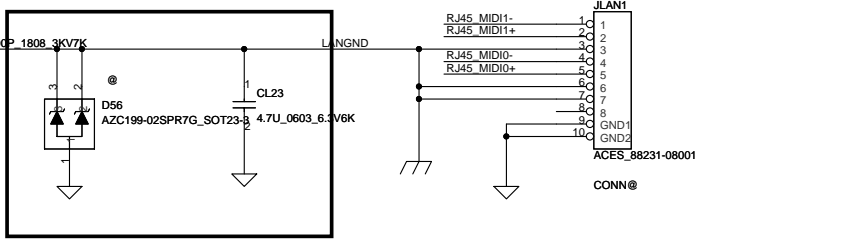
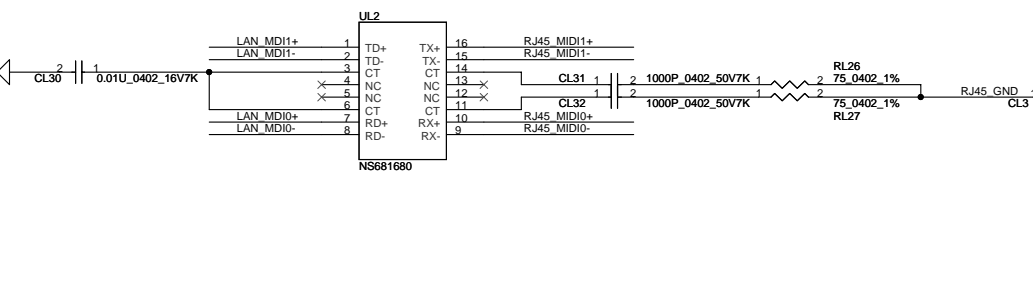
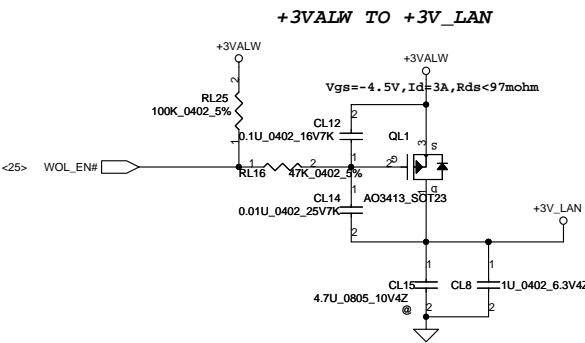
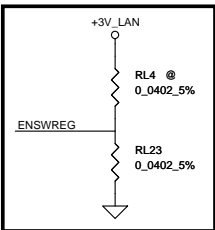
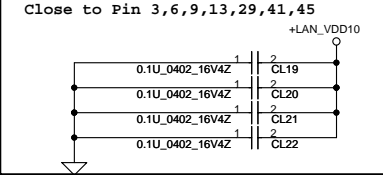
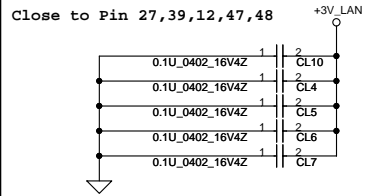
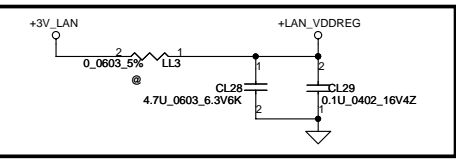
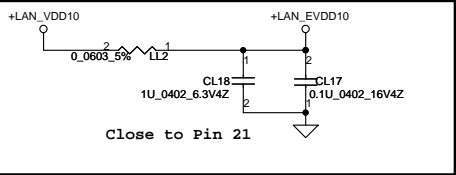
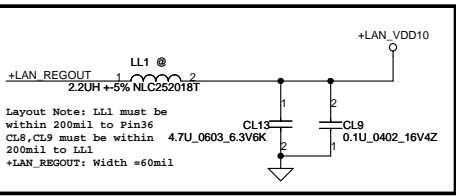
2011.04.20 Change to port 1



2011.04.26 Change control signal to EC_SWI#



3/10 Change CL13 0805-->0603



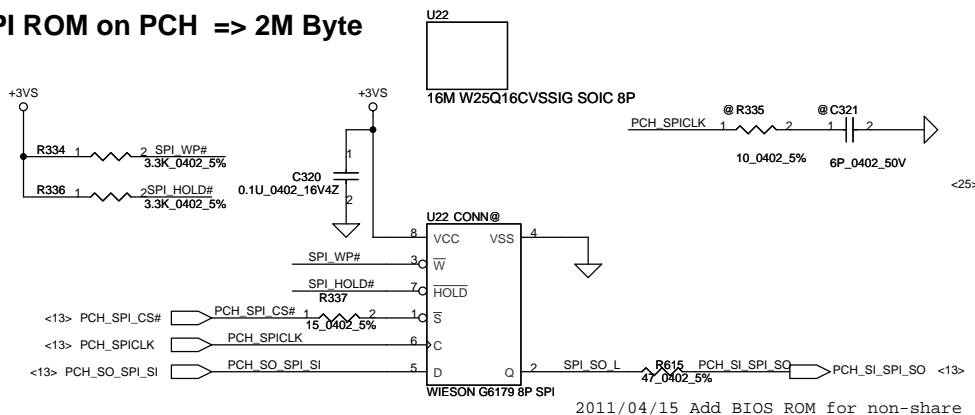
2011/04/18 Add D56 for ESD request

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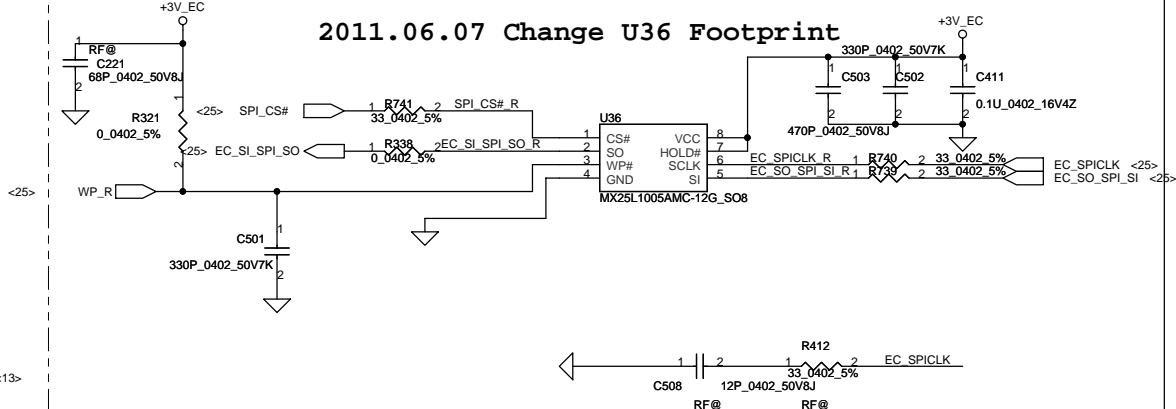


SPI ROM on PCH => 2M Byte

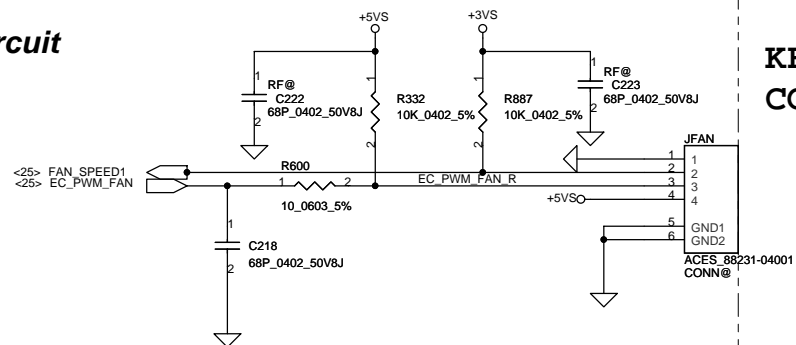


SPI Flash (1Mb*1)

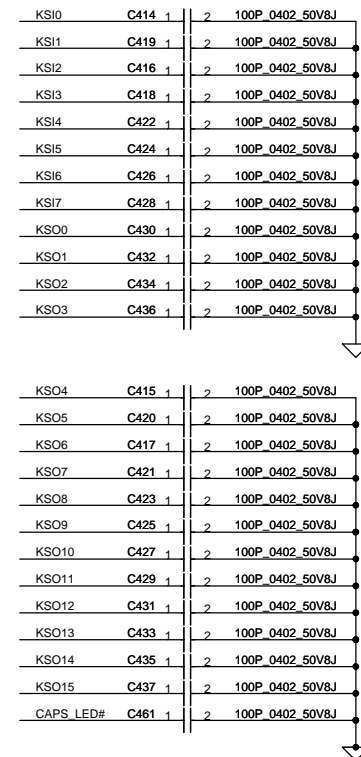
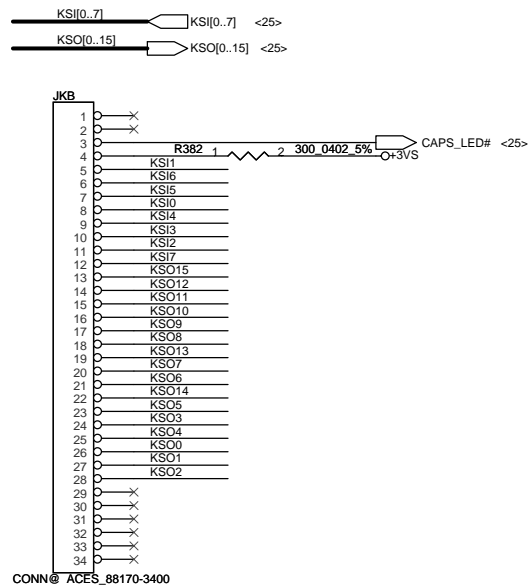
2011.06.07 Change U36 Footprint



FAN Control Circuit

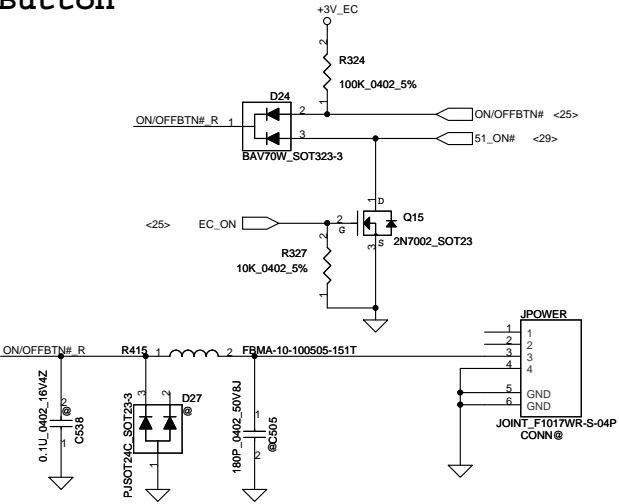


KEYBOARD
CONN.

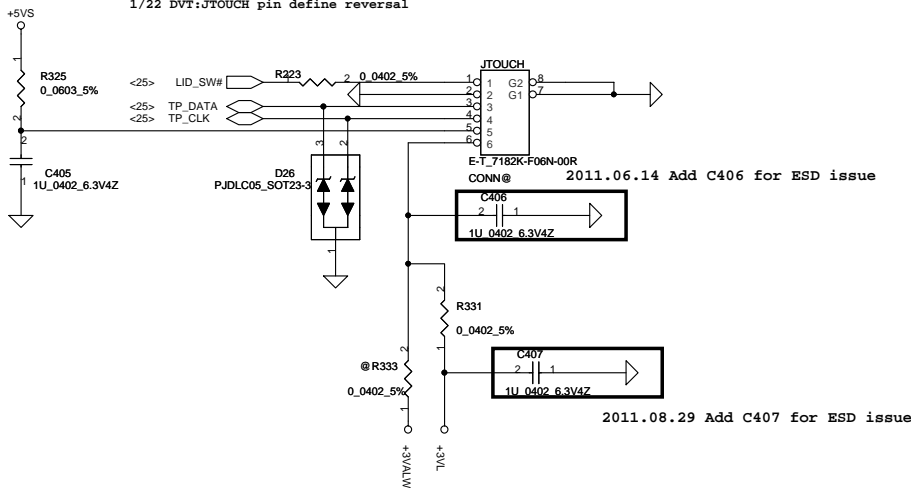


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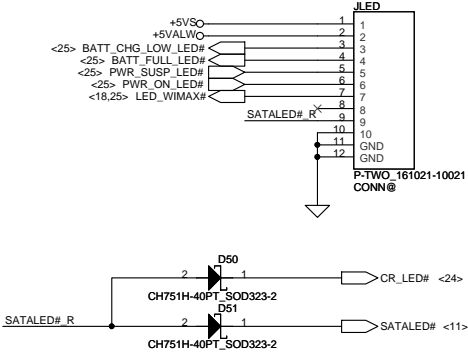
Power Button



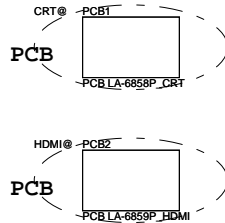
Touch/B Connector



LED Conn

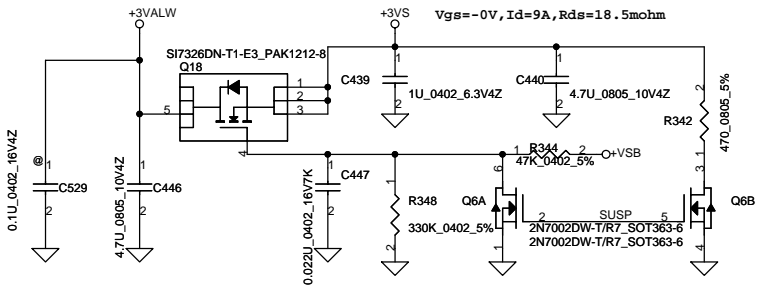


ISPD

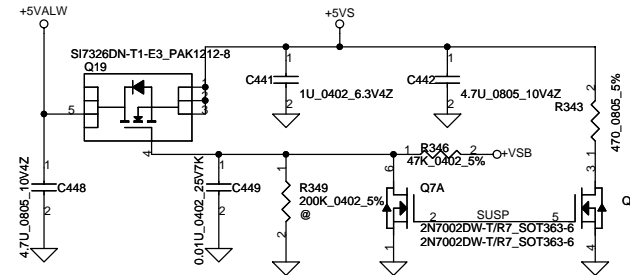


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+3VALW TO +3VS

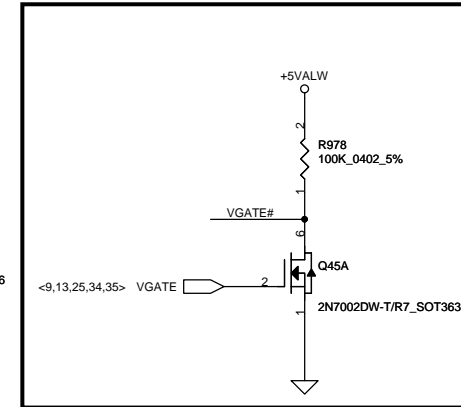
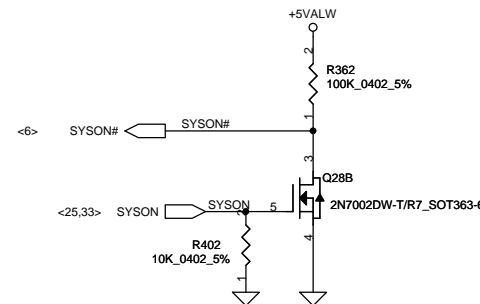
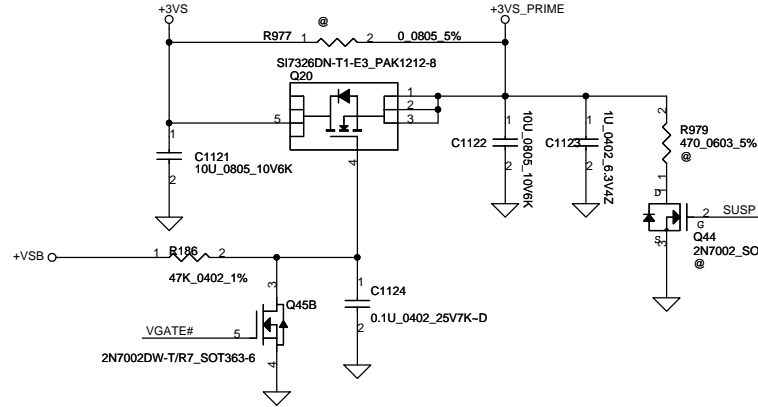


+5VALW TO +5VS

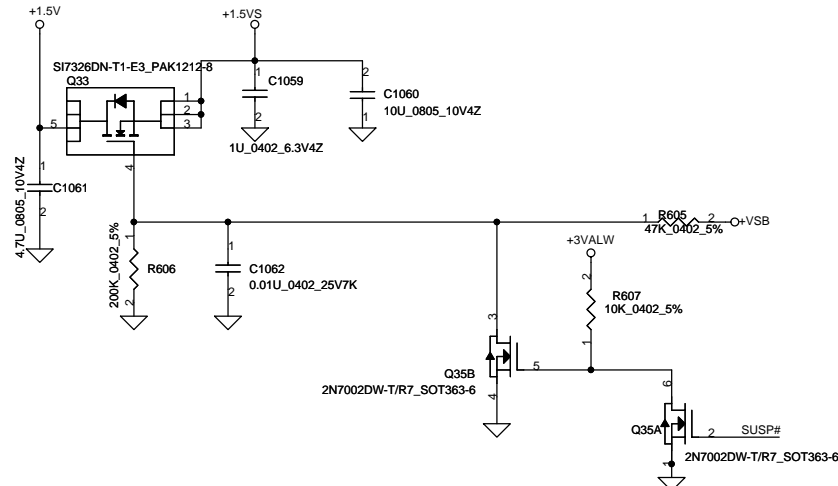


4/2 MP:For EMI ESD solution

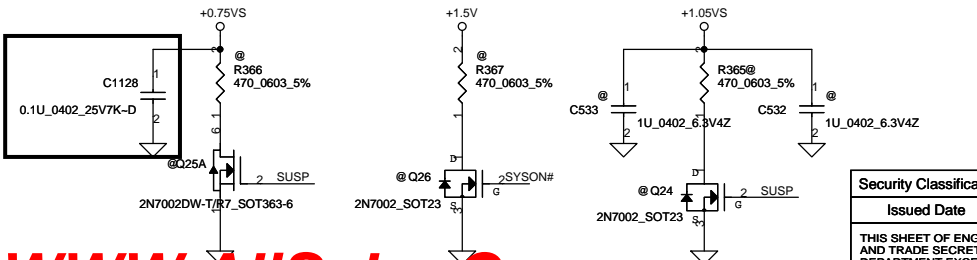
+3VS TO +3VS_PRIME



+1.5V TO +1.5VS



2011.06.14 Add C1128 for ESD issue



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DC301001M80

DC IN S1 1 2

5A_32V_S1206-H-5.0A

DC IN S2

PL1 SMB3025500YA_2P

PJP1

@ SINGA_2DW-0005-B03

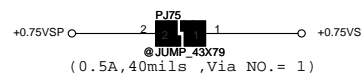
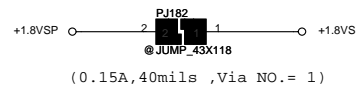
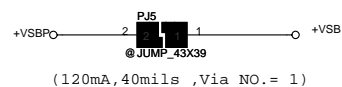
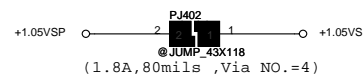
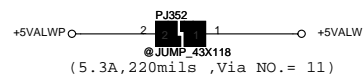
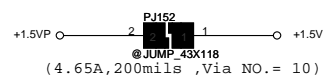
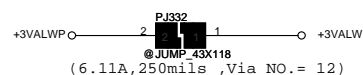
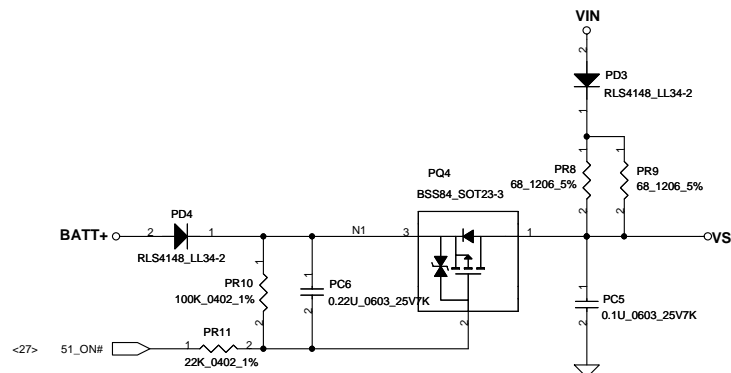
PC1 1000P_0402_50V7K

PC2 100P_0402_50V8J

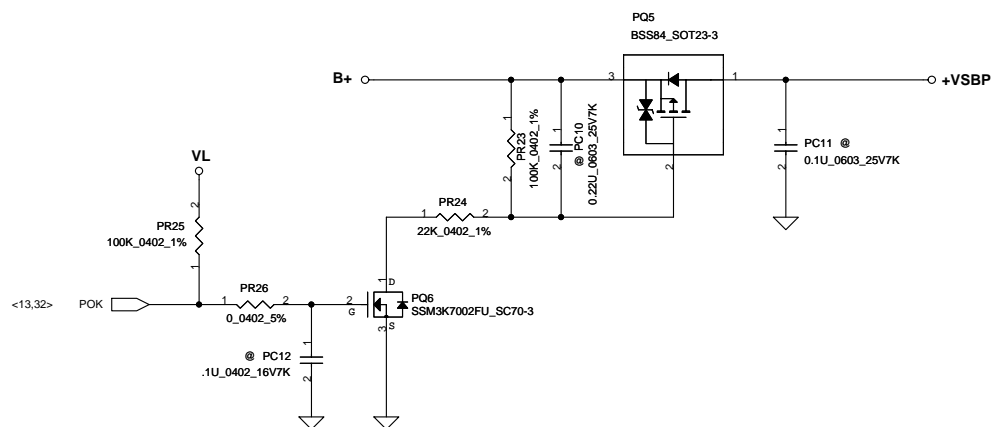
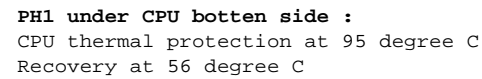
PC3 1000P_0402_50V7K

PC4 1000P_0402_50V8J

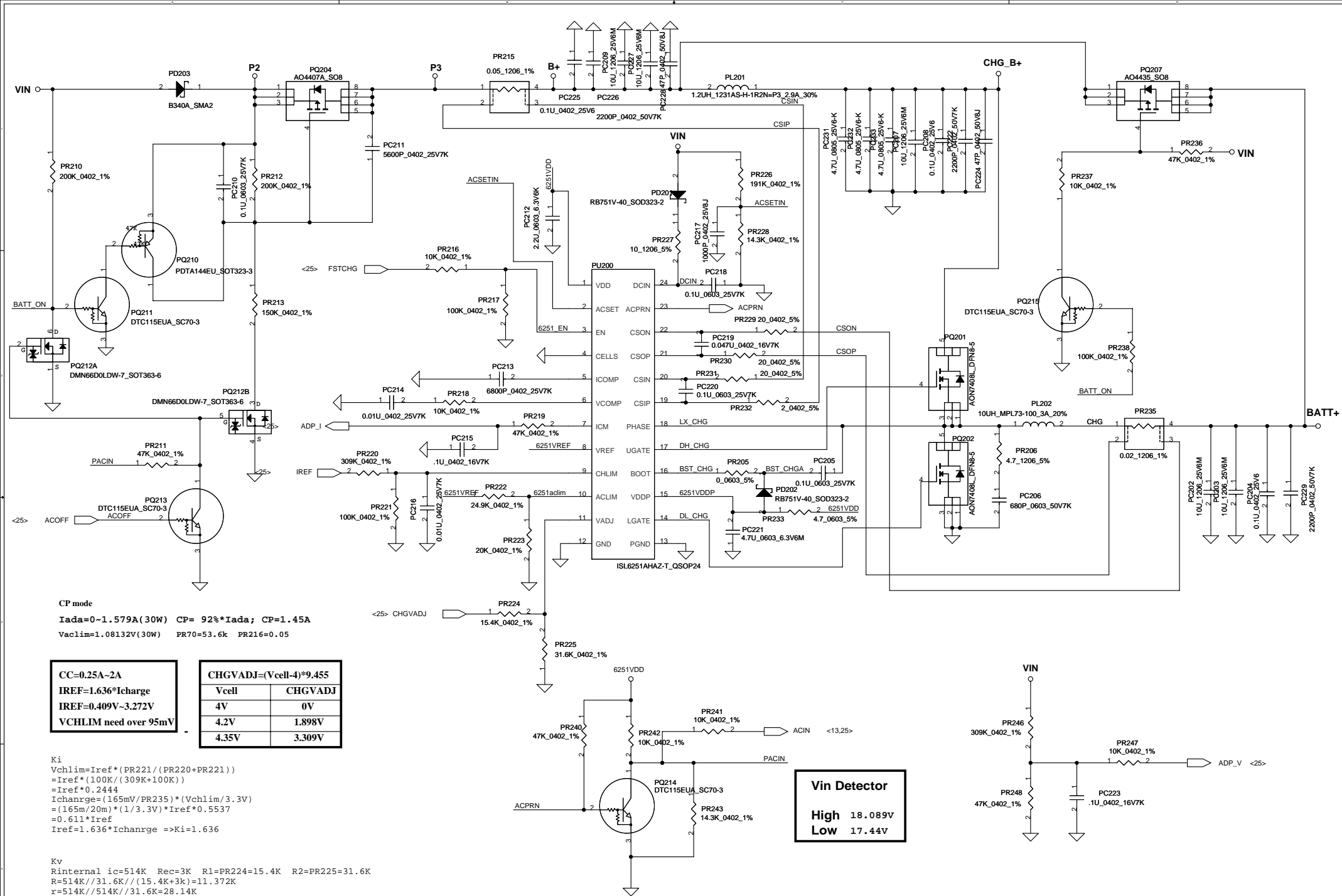
VIN



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CP mode
 $I_{ada}=0-1.579A(30W)$ $CP=92\% \cdot I_{ada}$; $CP=1.45A$
 $V_{aclim}=1.08132V(30W)$ $PR70=53.6k$ $PR216=0.05$

$CC=0.25A-2A$
 $I_{REF}=1.636 \cdot I_{charge}$
 $I_{REF}=0.409V-3.272V$
 V_{CHLIM} need over $95mV$

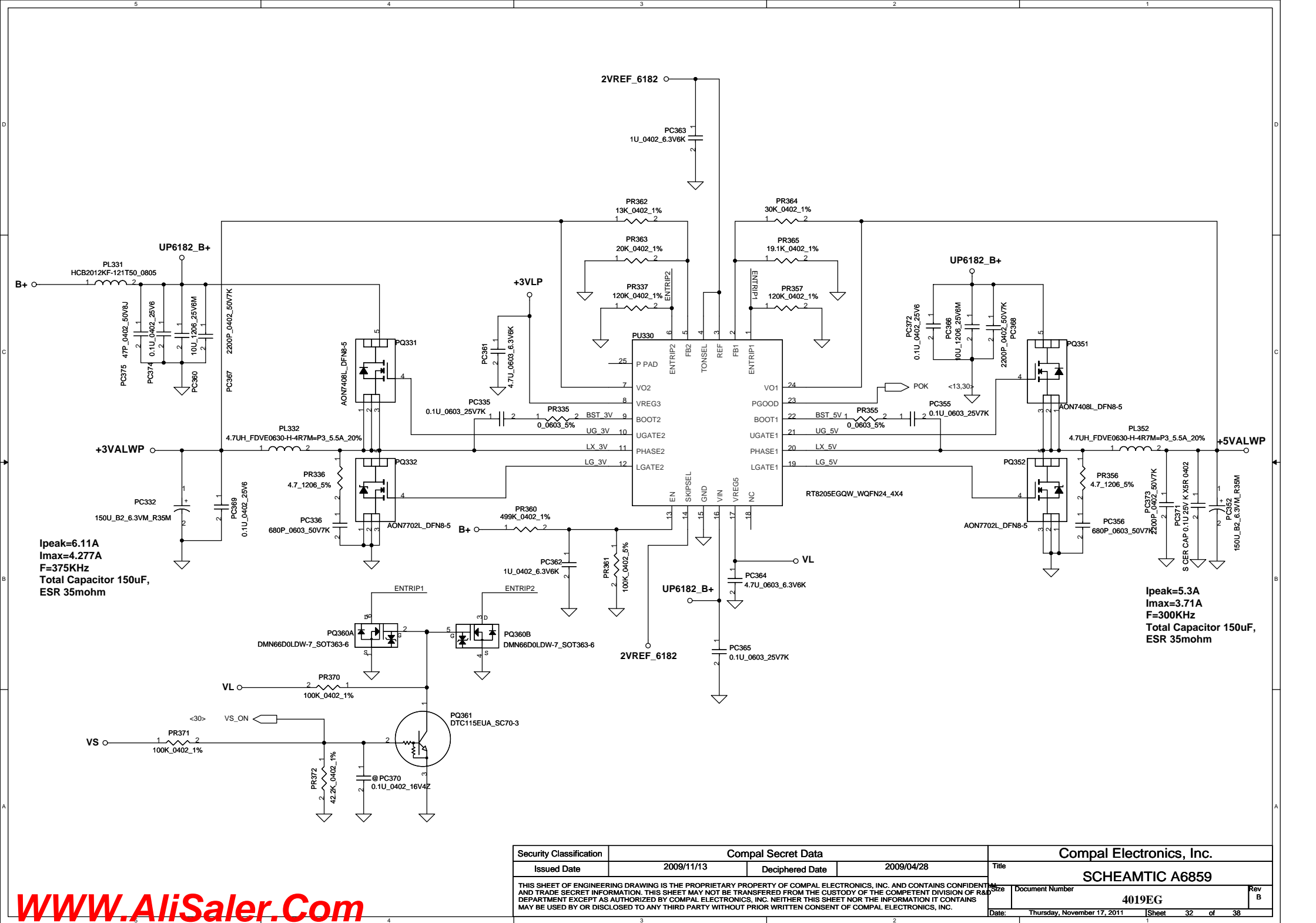
CHGVADJ=(Vcell-4)*9.455	
Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.309V

Ki
 $V_{chlim}=I_{ref} \cdot (PR221 / (PR220 + PR221))$
 $=I_{ref} \cdot (100K / (309K + 100K))$
 $=I_{ref} \cdot 0.2444$
 $I_{charge}=(165mV / PR235) \cdot (V_{chlim} / 3.3V)$
 $= (165m / 20m) \cdot (1 / 3.3V) \cdot I_{ref} \cdot 0.5537$
 $=0.611 \cdot I_{ref}$
 $I_{ref}=1.636 \cdot I_{charge} \Rightarrow Ki=1.636$

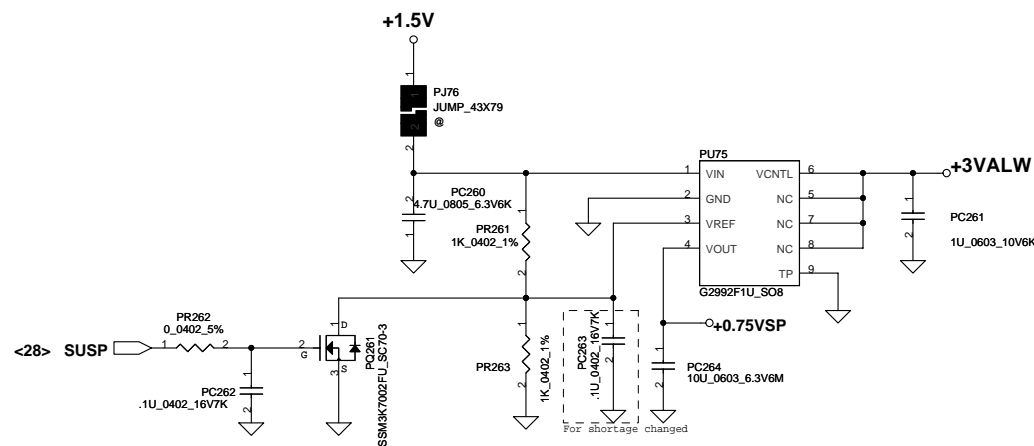
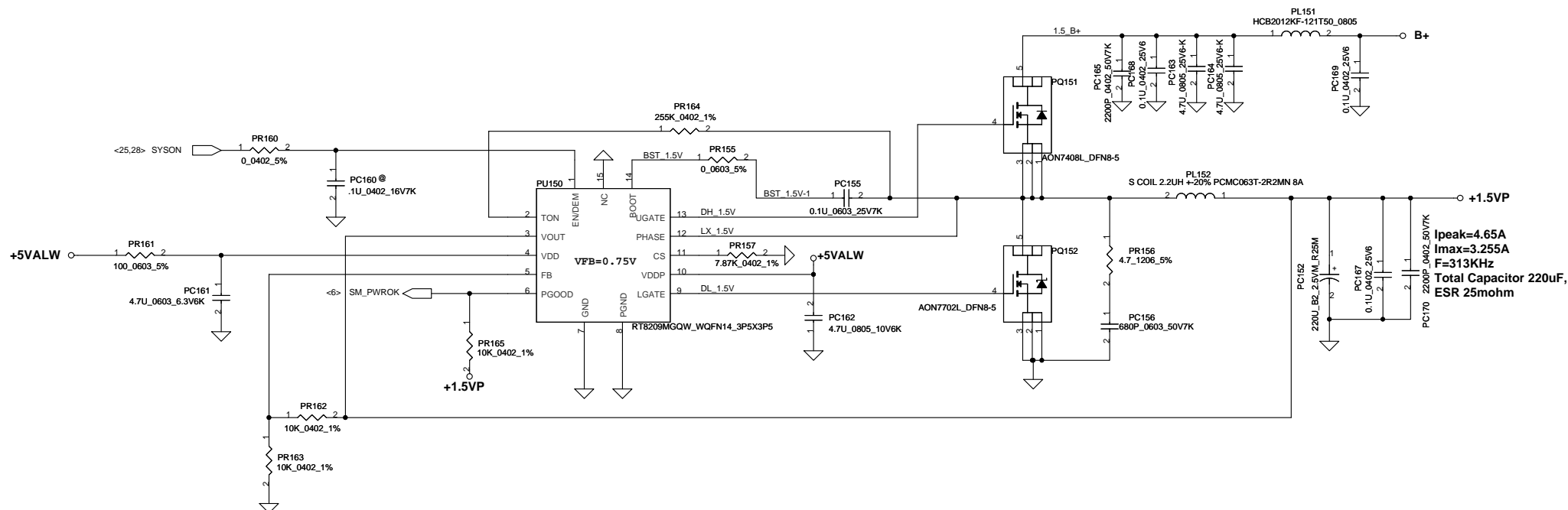
Kv
 Internal $i_c=514K$ $Rec=3K$ $R1=PR224=15.4K$ $R2=PR225=31.6K$
 $R=514K // 31.6K // (15.4K + 3k) = 11.372K$
 $r=514K // 514K // 31.6K = 28.14K$
 $V_{cell}=0.175 \cdot V_{adj} + 3.99V$
 $4.2V=0.175 \cdot V_{adj} + 3.99V \Rightarrow V_{adj}=1.2V$
 $V_{adj}=V_{ref} \cdot (R / (R + 514K)) + CALIBRATE \cdot (r / (r + 514K))$
 $1.1483=CALIBRATE \cdot 0.6046 \Rightarrow CALIBRATE=1.899$
 $1.899=(4.2 - (V_{cell} + A \cdot 0.175)) \cdot Kv \Rightarrow (4.2 - (4.2 + A \cdot 0.175)) \cdot Kv$
 $A=V_{ref} \cdot (R / (R + 514K)) = 0.052$
 $K1=4.5$

Vin Detector
 High 18.089V
 Low 17.44V

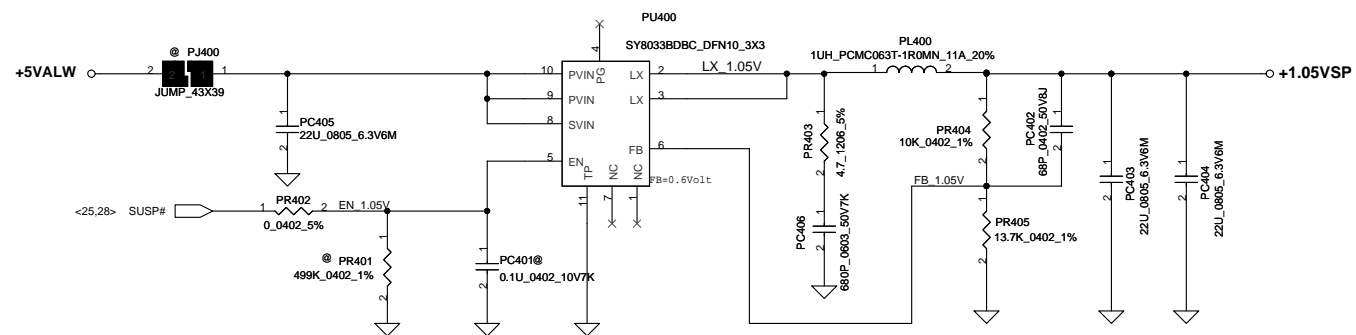
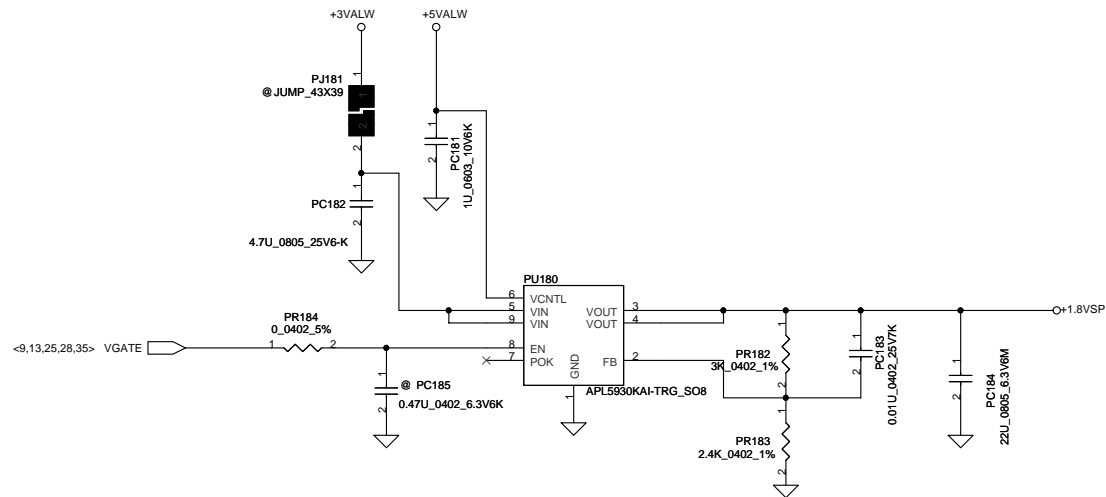
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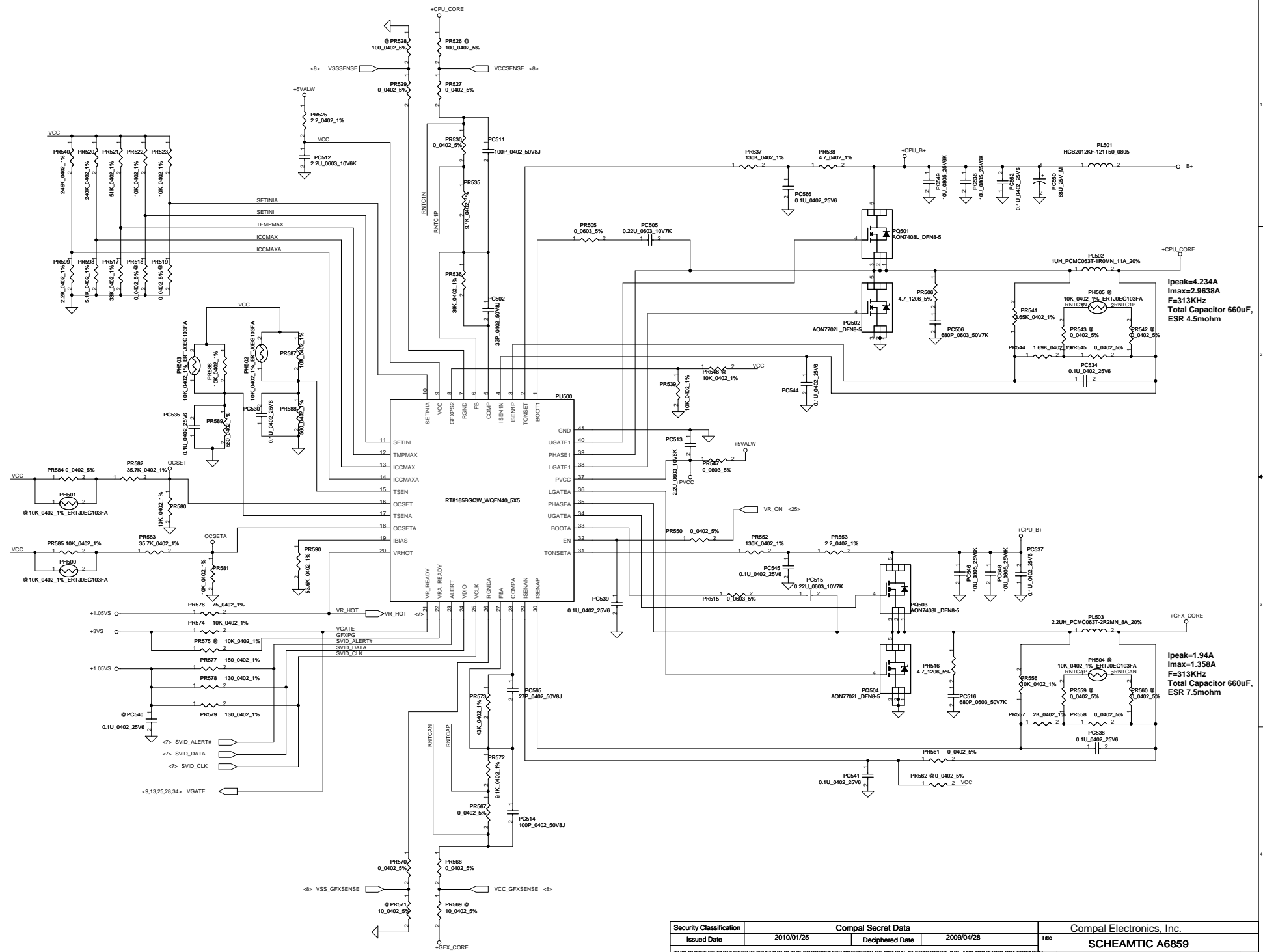
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Ipeak=1.8A
ILIM = 1.26A
F=1MHz
Total Capacitor 330uF, 9mohm

Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,
SY8035 is for 5A loading , let LX shape can bigger!!

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PIR (Product Improve Record)

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	04/ 26	06	Delete C948,C949,C950,C951	ES2 CPU only support 2 pairs DMI
02.	04/ 26	06	Add DDR_A_MA15 signal in CPU side	Cedar Trail platform supports MA0-MA15 total sixteen address signals
03.	04/ 26	07	Reserve 0 ohm for DDC_SCL / SDA , HPD, BREF1P5V, BREFREXT connect to GND.	Follow Intel V1.0 check list to disable HDMI
04.	04/ 26	07	Add CRT DAC,SYNC signals and add RV155,RV156,RV157 150 ohm pull down resistor for CRT DAC signal.	Follow Intel V1.0 check list to enable RGB I/F
05.	04/ 26	08	Reserve 0 ohm for VCCADP / VCCADP_SFR connect to GND	Follow Intel V1.0 check list to disable HDMI
06.	04/ 26	08	Add R1004,C166 for +VCCDIO / R535,C1125 for +VCC_CRT_DAC	Follow Intel V1.0 check list to enable RGB I/F
07.	04/ 26	10	Add MA15 signal for SODIMM connector	Cedar Trail platform supports MA0-MA15 total sixteen address signals
08.	04/ 26	11	Stuff R544	System will change to non-share ROM design, PCH STRAP2/1 will be 01
09.	04/ 26	12	Change PCIe port arrangement	Follow BIOS team's request to re-arrang PCIe port for power saving.
10.	04/ 26	13	Use BOM option for R931,R932,R933,R934	Follow Intel V1.0 check list to disable HDMI
11.	04/ 26	13	Add J2 and C1087 for PCH GPIO12	BIOS will use GPIO12 for clean password function.
12.	04/ 26	13	Add R566,R567,R618 10K pull high resistors for PCH SPI I/F	System will change to non-share ROM design
13.	04/ 26	15	Add CRT circuit	Follow Intel PDG and V1.0 check list to implement CRT circuit
14.	04/ 26	19	Change USB charger(US1) solution to MAX14566B	Follow A51 common design
15.	04/ 26	19	Reserve US2 bus switch	Support BIOS team's new debug card.
16.	04/ 26	19	Change US4 USB power switch to 2A	Support USB charge V1.1 SPEC--->support 1.8A
17.	04/ 26	23	Change LOM_WAKE# control signal to EC_SWI#	LOM WAKE# will connect to PCH directly and change net name to "EC_SWI#"
18.	04/ 26	25	Change KBC to KB930/KB9012	Follow EC team KB930/KB9012 common design
19.	04/ 26	26	Add U22 -->2MB SPI ROM	System will change to non-share ROM design
20.	04/ 28	18	Reserve 0 ohm and test points in JGPS pin1/3/5/44/46/51	Cougar 2.0 will support new 3G/LTE module
21.	04/ 29	25	Delete C211,C212,C216,C217	RF team has no necessity
22.	04/ 29	07	Delete 220p caps for sideband signals.	EMC team has no necessity
23.	04/ 29	09	Delete C940,C941	RF team has no necessity
24.	04/ 29	09	Delete C1067,C1066	RF team has no necessity
25.	04/ 29	09	Reserve R305,C392 for SMBus_CLK	Reserve R-C for RF team's requirement
26.	04/ 29	17	Delete C227,C228,C290,C230,C231,C232,C1074,C1075	RF team has no necessity
27.	04/ 29	18	Delete C307,C298,C297	RF team has no necessity
28.	05/ 03	07	Add R984 0 ohm resistor for XDP pin17	Reserve 0 ohm for XDP when XDP connector no use.
29.	05/ 04	16	Change Q42,Q43 to dual package	Save layout space and cost
30.	05/ 06	07	Add R989 (0 ohm) for XDP signal	Reserve 0 ohm for XDP when XDP connector no use.
31.	05/ 10	15	Delete D53,F1,C1110	Share 5V with CRT circuit.
32.	05/ 10	07	Change XDP un-define net name	Follow naming rule

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	06/ 07	07	Remove XDP connector	XDP debug port is no necessary in PVT
02.	06/ 07	08	Keep +VCCADP_1.05, +VCCADP_SFR power rail even disable DDI interface	Intel correct their DDI disable guideline
03.	06/ 07	26	Change U36 Symbol and footprint	Fix DFB issue
04.	06/ 10	13	Change J1 to JCMOS, J2 to JPW	Follow A51 jumper naming rule
05.	06/ 10	19	Remove US2 USB bus switch	PVT won't reserve USB debug port
06.	06/ 14	08	Stuff 1u (C1007,C1008,C1009) on GFX_CORE	To solve ESD issue
07.	06/ 14	28	Add 0.1u (C1128) on +0.75VS power rail	To solve ESD issue
08.	06/ 14	10	Add 0.1u (C116) on +0.75VS power rail	To solve ESD issue
09.	06/ 14	10	Add 0.1u (C119) on +1.5V power rail	To solve ESD issue
10.	06/ 14	10	Add 0.1u (C406) on +1.5V power rail	To solve ESD issue
11.	06/ 14	27	Add 1u (C406) on touch pad power rail	To solve ESD issue
12.	06/ 15	13	Change PCH SPI I/F pull high to +3VS	To solve S3/S5 +3VS power plan leakage issue
13.	06/ 16	20	Stuff 0.1u (C280) on +3VS power rail	To solve ESD issue
14.	06/ 18	07	Add R1009, R1010 for DDI1_DDC_SCL/SDA	Follow Intel DDI disable guideline

PIR (Product Improve Record)

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3

NO DATE PAGE MODIFICATION LIST				PURPOSE
01.	06/ 29	09	Swap CLK Gen output for CPU_SCDREFFCLK and CPU_DREFCLK	Intel recommend CPU_SSCDREFFCLK use SSC CLK

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0

NO DATE PAGE MODIFICATION LIST				PURPOSE
01.	08/ 29	07	Change R975 from 10ohm to 0 ohm	Follow Intel CRB design.
02.	08/ 29	25	Un-stuff R312,R313	KS01,KS02 of KB930 don't need to pull high.
03.	08/ 29	27	Add 1u(C406) on touch pad power rail.	To solve ESD issue

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2011/06/14		32	PR336, PR356 to 1206 4.7ohm; PC336, PC356 to 0603 680pF	For EMI Solution
2011/06/14		35	PR526, PR528, PR569, PR571 to @ PR506, PR516 to 1206 4.7ohm; PC506, PC516 to 0603 680pF	For EMI Solution
2011/06/14		33	PU150 change to RT8209MGQW	
2011/06/14		33	PR157 change to S RES 1/16W 7.87K +-1% 0402	For OCP Solution
2011/06/14		35	PC550 to @	Reserve PC550 location and change it to 5.3mm cap (SF000003Z00) for ME solution
2011/06/21		35	PC536 to 42.2K	Change PR536 to 42.2Kohm to meet Cedar Trail loadline spec
2011/06/27		35	PH505, PR542, PR543, PH504, PR559, PR560 to @ PR545, PR558, PR530, PR567 to 0ohm PR541 to 3.62K, PR544 to 1.69K, PR556 to 10K PR557 to 2K, PR536 to 39K	For Cedar Trail loadline spec
2011/06/27		35	PR582, PR583 to 35.7K	For CPU & GFX OCP Solution
2011/06/27		35	PL503 to 2.2uH	Base on GFX_Core ripple & dynamic test result
2011/06/27		35	PR584 to 0_0402_5%	For AP Code material
2011/11/1		29	PF1 change to SART 5A_32V_S1206-H-5.0A	For burn out issue
2011/11/1		30	PF2 change to Cooper 7A_32V_TR/3216FF-R	For burn out issue
2011/11/1		32	PU330 change to RT8205EGQW	For burn out issue
2011/11/1		35	PC550 change to Lelon 68uF 5.3H	For acoustic issue

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